

IST calibration Plan

Babak Abi

04/04/14

IST Calibration Plan

- **Bad Chip/Channels list**
 - Tracked weekly after each major firmware update and check any changed in permanent Dead Chip/Channels
 - Including the DAQ (Tonko's) generated list of mis-configured chips to Study (it is run-by-run) (file: DAQMAN@/net/ist01/RTScache/ist_apv_bad.txt)
 - Creating new data DB offline based on mis-configured (run-by-run).
- **Generate istPedNoise noise Db table daily and after each major firmware update.**
 - Using Pedestal/Noise from Tonko's files (pedestal_tcd_only produce daily)
 - Using pedAsPhys for Common mode noise .
- **Starting systematic study :**
 - Channels' ADC to electron charge gain translation. (istGain)
 - Offline reconstruction Cuts (istControl)

Back Up slides

Dead Chip/Channels procedure

- Goal is to make Permanent dead Chip/Channels tables based on all run.
 - 209 Cosmic runs is used plots at :
 - http://www4.rcf.bnl.gov/~babakabi/public_html/plots/index.htm
 - I. Pedestal/noise per ladders (3rd Timebin)
 - II. Pedestal/Noise/ComModeNoise for All time bins .
 - III. Pedestal/Noise Stability for time bins 0 to 5 from Cosmic runs days 32 to 40

- General Characteristics of Silicon Strip Modules

1) Pedestal of Strip i from M events :

$$p_i = \frac{1}{M} \sum_{j=1}^M r_{ij} ,$$

2) Pedestal-noise of Strip i from M events

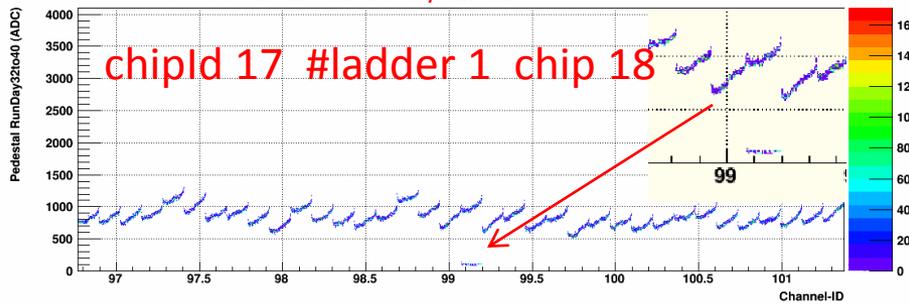
$$\sigma_i = RMS(r_{ij}) = \sqrt{\frac{1}{M} \sum_{j=1}^M (r_{ij} - p_i)^2}$$

3) Common mode offset (noise) of APV chip event j .

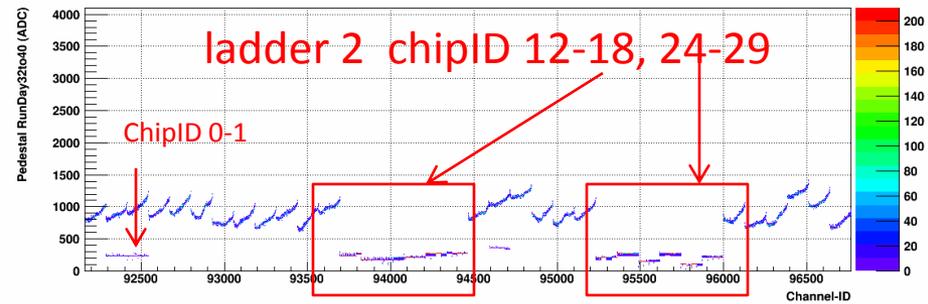
- The common mode noise is the RMS of the common mode distribution

$$CM_j = \frac{1}{128} \sum_{i=1}^{128} (r_{ij} - p_i)$$

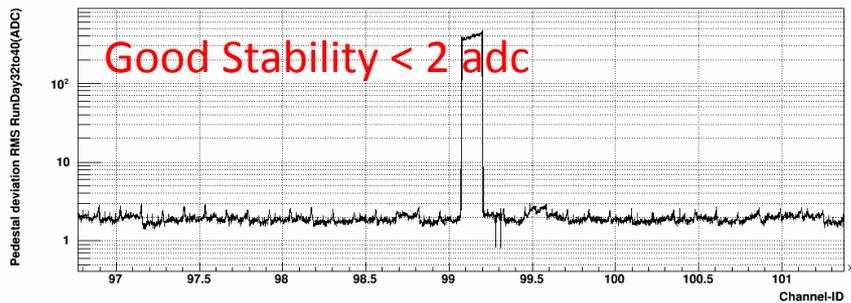
Ladder #1 Time-bin1 Pedestal distribution/allruns



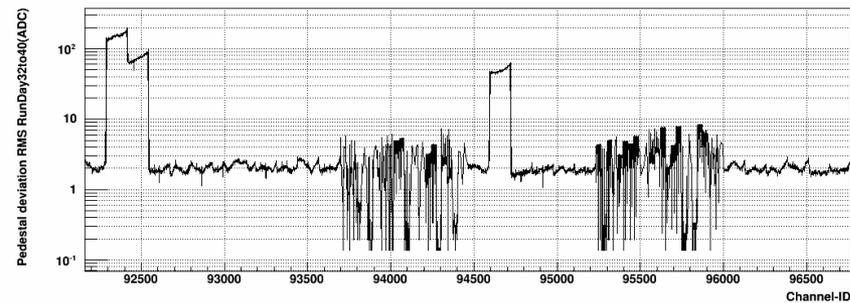
Ladder #2 Time-bin1



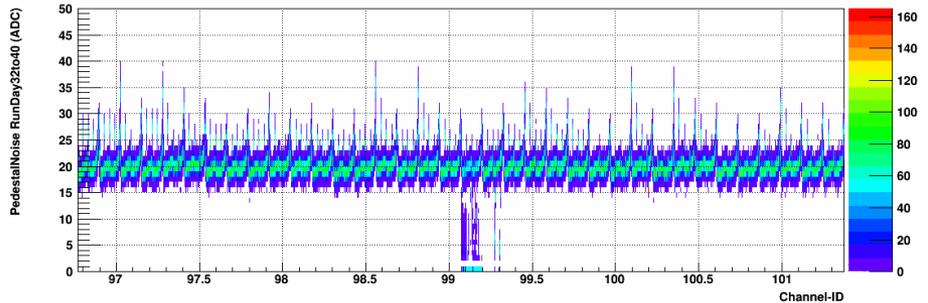
Ladder #1 Time-bin1 Pedestal deviation rms/allruns



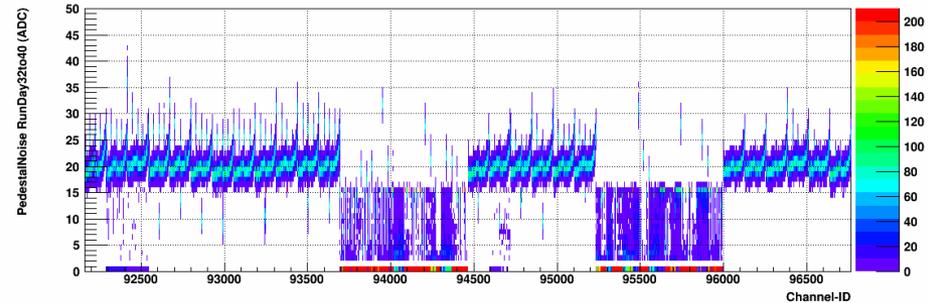
Ladder #2 Time-bin1



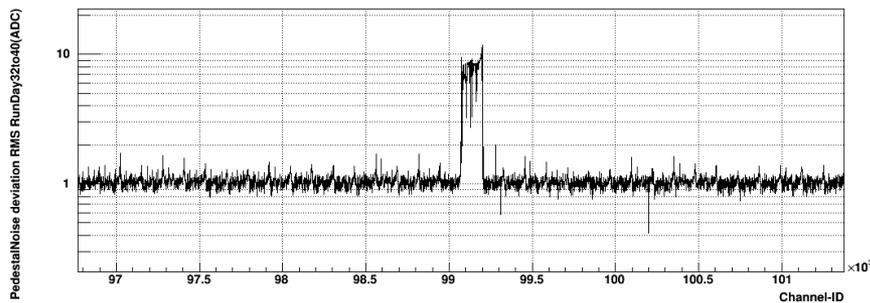
Ladder #1 Time-bin1 Pedestal -Noise distribution/allruns



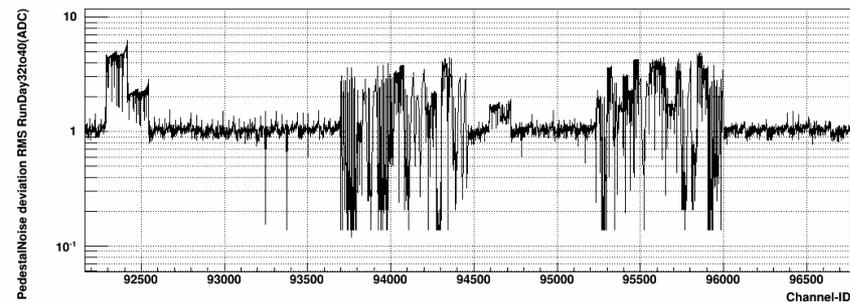
Ladder #2 Time-bin1



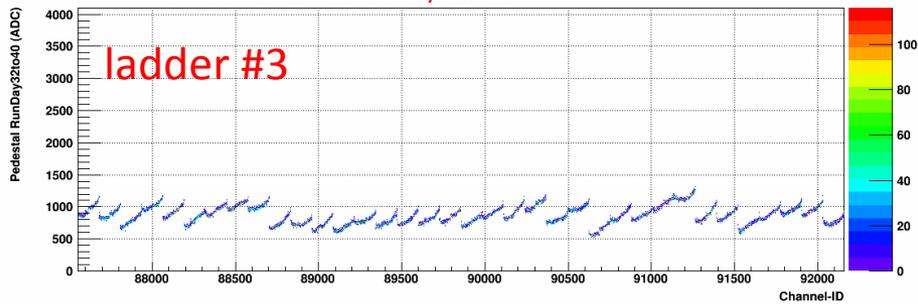
Ladder #1 Time-bin1 Pedestal -noise deviation rms/allruns



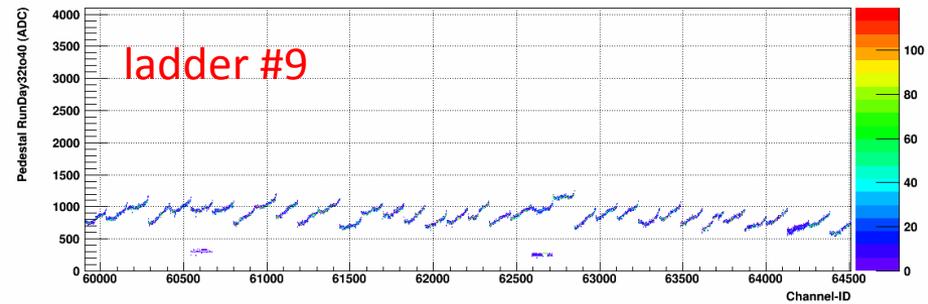
Ladder #2 Time-bin1



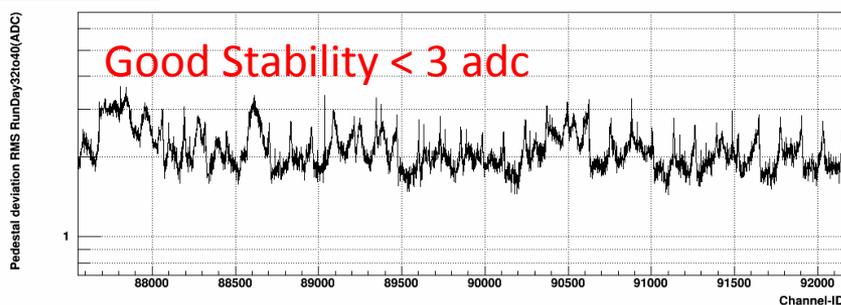
Ladder #3 Time-bin1 Pedestal distribution/allruns



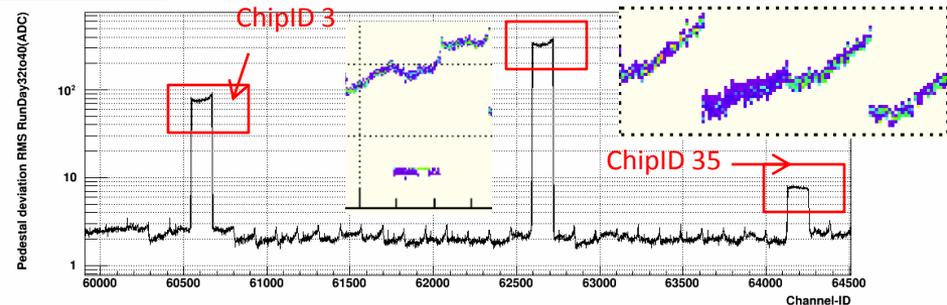
Ladder #9 Time-bin1



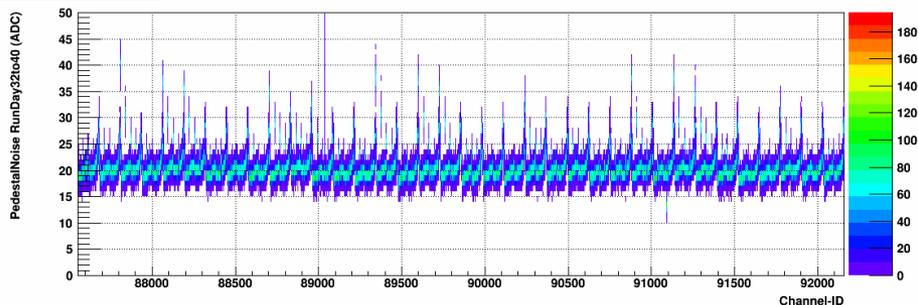
Ladder #3 Time-bin1 Pedestal deviation rms/allruns



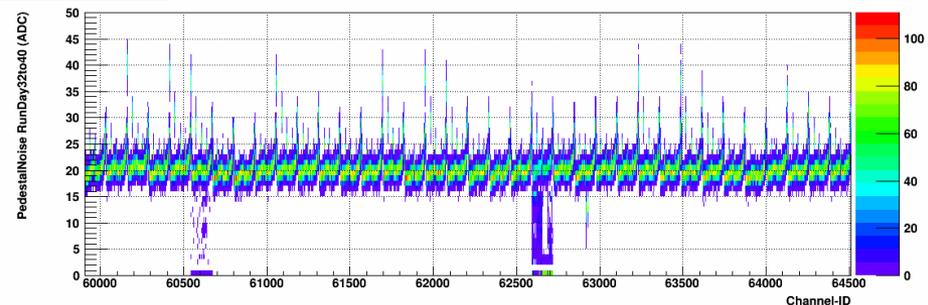
Ladder #9 Time-bin1



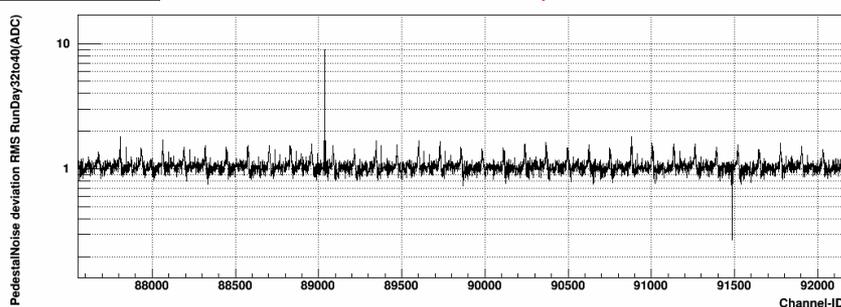
Ladder #3 Time-bin1 Pedestal -Noise distribution /allruns



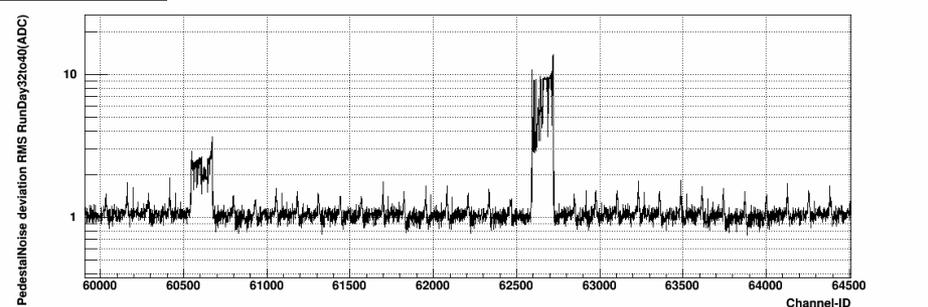
Ladder #9 Time-bin1



Ladder #3 Time-bin1 Pedestal -noise deviation rms/allruns



Ladder #9 Time-bin1

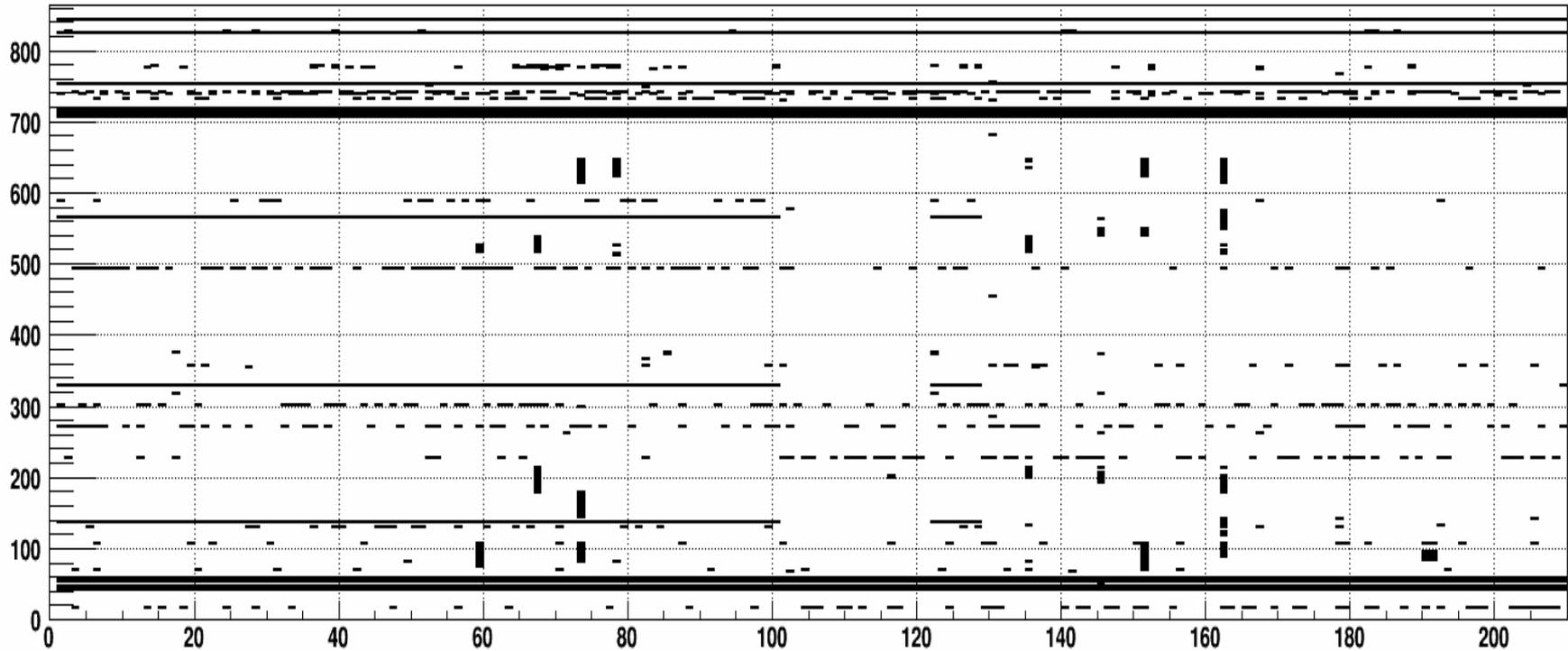


Distribution of Bad Chip/channels current scheme

- Latest results at : (would be updated and ,ore detaile)

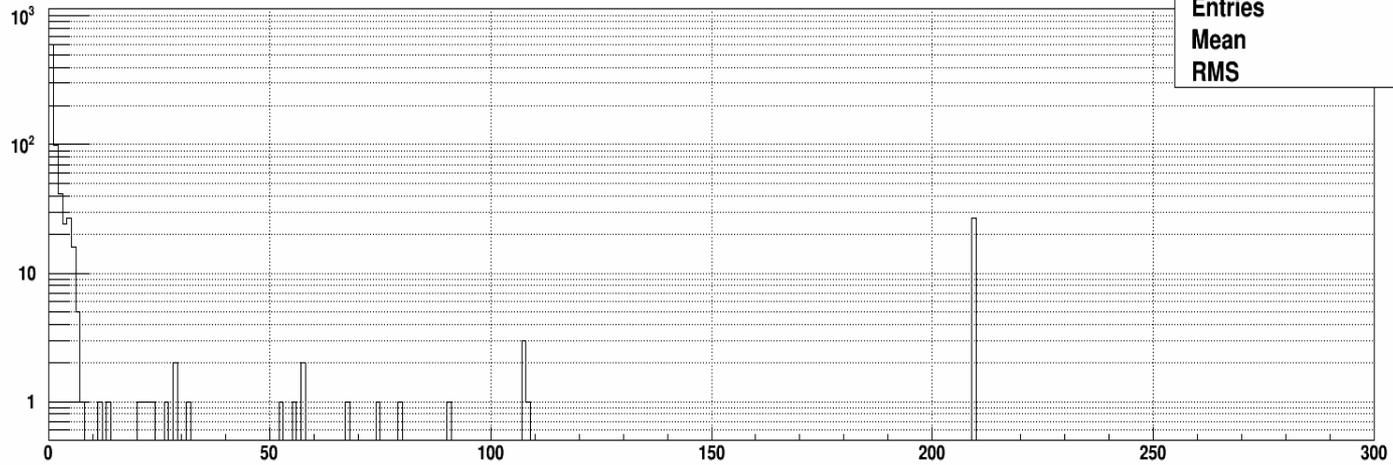
http://www4.rcf.bnl.gov/~babakabi/public_html/plots/BCC/bcc.htm

DeadChips vs Runs



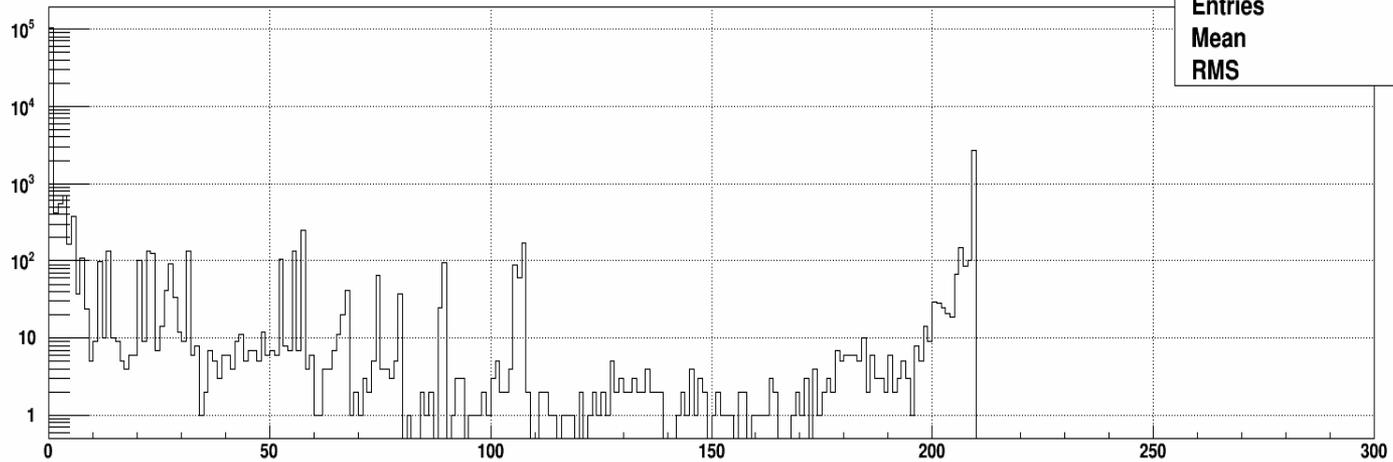
Rate failure for 209 runs

Chips failed



h_chipsNfailed	
Entries	864
Mean	8.453
RMS	37.38

#Channels failed



h_channelsNfailed	
Entries	110592
Mean	7.523
RMS	36.55