



Inputs:

PR and CLR can be used to force the state of the outputs to a HIGH or LOW state
 DAV* is a hardware signal from the GLINK circuit indicating DataAvailable - Valid data if LINKRDY* is also active indicating startup sequence is complete
 LINKRDY* is a hardware signal from the GLINK circuit indicating locked operation - (Valid data)
 STAT0 is a hardware signal from the GLINK circuit indicating correct state machine recovery of the clk strobe (Enable Data Transmission on Tx)
 MODE_BITS[0..7] and the USER_BITS[0..2] are all data from the GLINK specifying the operating mode of the FEM / ROC cards
 MB_BCLK is a data bit "beam clock" that changes every forth STRBOUT from the GLINK
 TMODE_EN is a data bit from the GLINK that specifies whether to decode the mode bits or hold the last valid state - (Timing Mode Enable)
 MB_LVL1_ACPT is a data bit that indicates Data is to be saved and sent to the DCM for processing

Outputs:

BCLK - Beam Clock mode bit gated with STAT0 - used to drive all mode control logic
 RUN - Indicates the normal run mode
 CLR_FIFO - Reset all FIFO's
 CLR_CNTR - Reset all counters: Beam clock and event
 FEM_RST - General Reset for FEM Card
 DMUX_RST - Hold outputs from the DELAY MUX's
 S_FUN0 - Not yet defined - Spare output
 S_FUN1 - Not yet defined - Spare output
 PULSER - Fires local analog pulser
 ALIGN - Alignment timing marker
 MODE_BIT_ERR - Indicates the reception of an invalid mode-bit combination
 ARCNET_RST - Reset Arcnet
 FEM_SELF_TEST - Diagnostic Mode
 LVL1_ACPT - Data is to be saved and sent to the DCM for processing
 ENDAT - Enable Data transmission to the DCM

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