

# STATUS REPORT ON THE MAPS DETECTORS FOR THE WARM AND THE SUPERCONDUCTOR OPTIONS OF THE FLC

## OUTLINE:

▶▶ INTRODUCTION OF MAPS TECHNOLOGY

▶▶ WHERE MAPS ARE, AND PLANS FOR USE AT VX  STAR

▶▶ HOW FAR TO FULFIL FLC REQUIREMENTS (,  $\sigma$ ,  ...)

▶▶ RDOUT STRATEGIES FOR WARM & COLD FLC

▶▶ DEVELOPMENT OF FAST RDOUT CIRCUITS

▶▶ CONCLUSIONS + FUTURE R&D

Grzegorz Deptuch, LEPSI, Strasbourg, France

*speaking for IReS-LEPSI collaboration: A.Besson, G.Claus, C.Colledani, G.Deptuch, M.Deveaux, W.Dulinski, A.Gay, G.Gaycken, Yu.Gornushkin, D.Grandjean, F.Guilloux, S.Heini, A.Himmi, Ch.Hu, K.Jaaskelainen, H.Souffi-Kebbat, M.Szelezniak, I.Valin, M.Winter*

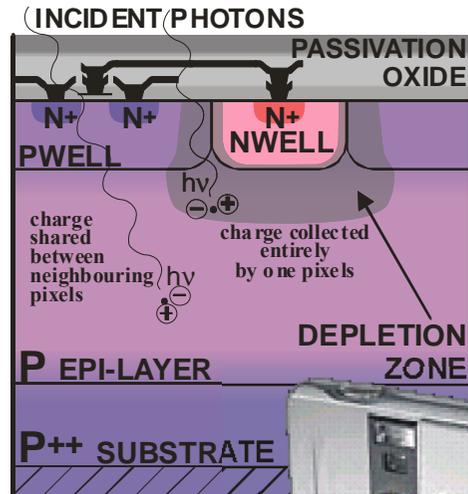
*and M6/M8 DAPNIA: Y.Degerli, N.Fourches, F.Orsini, P.lutz*





# INTRODUCTION OF MAPS TECHNOLOGY

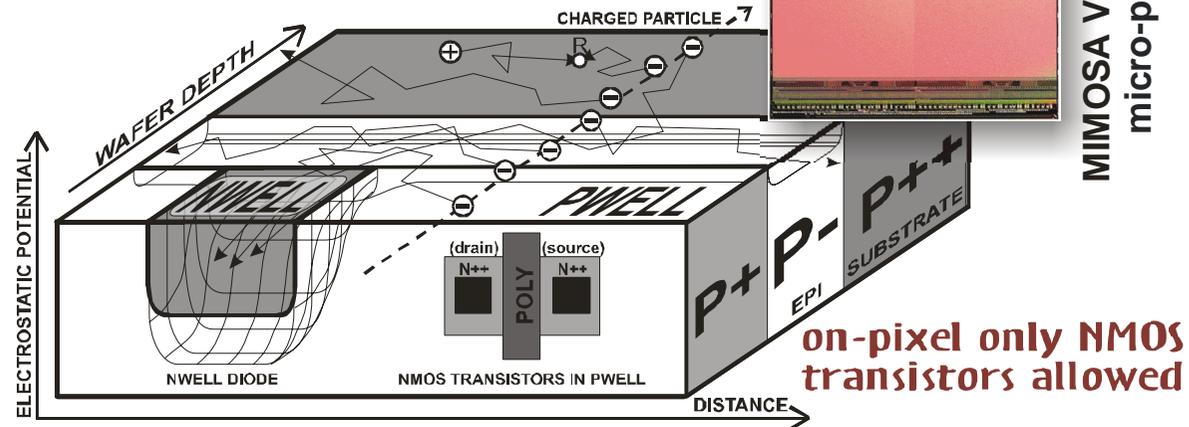
## From digital photography



'warmest' colour = highest electric potential in the device



## to charged particle detection



MIMOSA V 1x10<sup>6</sup> pixels micro-photograph

## Monolithic Active Pixel Sensors (MAPS)

The detector is a standard VLSI chip. The active element is a thin **moderately doped** silicon layer, operated **undepleted**. The readout electronics is seated on top of this layer. The built-in potential, resulting from differences in doping, **screens** the detector from the electronics parts and **confines** the charge diffusing to the readout electrodes. The charge collectors are **n-well/p-epi** (substrate) diodes. Only NMOS transistors are used for in-pixel readout electronics, but full CMOS electronics is used on the detector periphery.

### MAPS ADVANTAGES:

decoupled charge sensing and signal transfer (improved radiation tolerance, random access, etc.), small pitch (high tracking precision), low amount of material, fast readout, moderate price, SoC, etc.

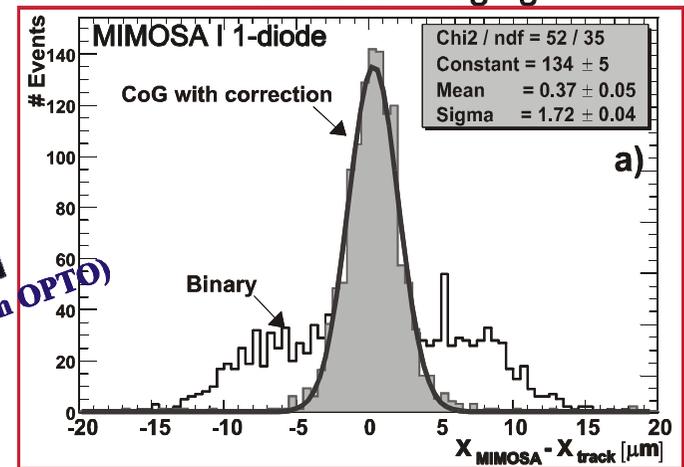




# INTRODUCTION OF MAPS TECHNOLOGY

**first MAPS:**

**M**APS detectors are developed at IReS-LEPSI since 1999 for future vertex detectors (very high granularity + minimal material budget) and biomedical imaging.

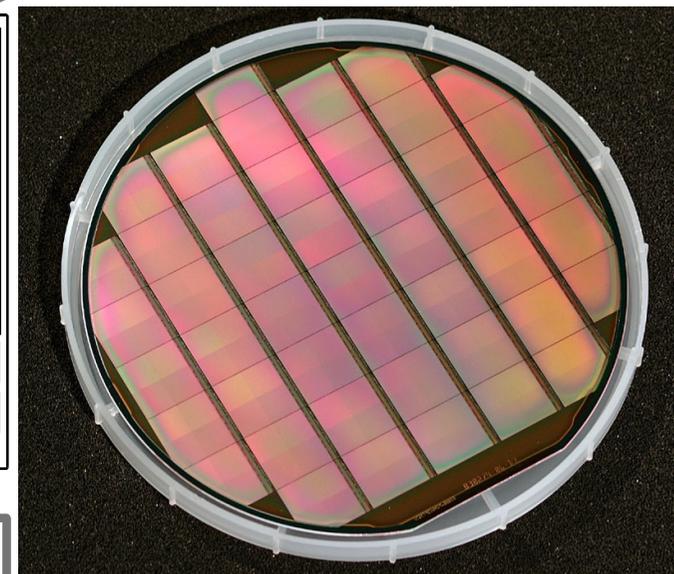
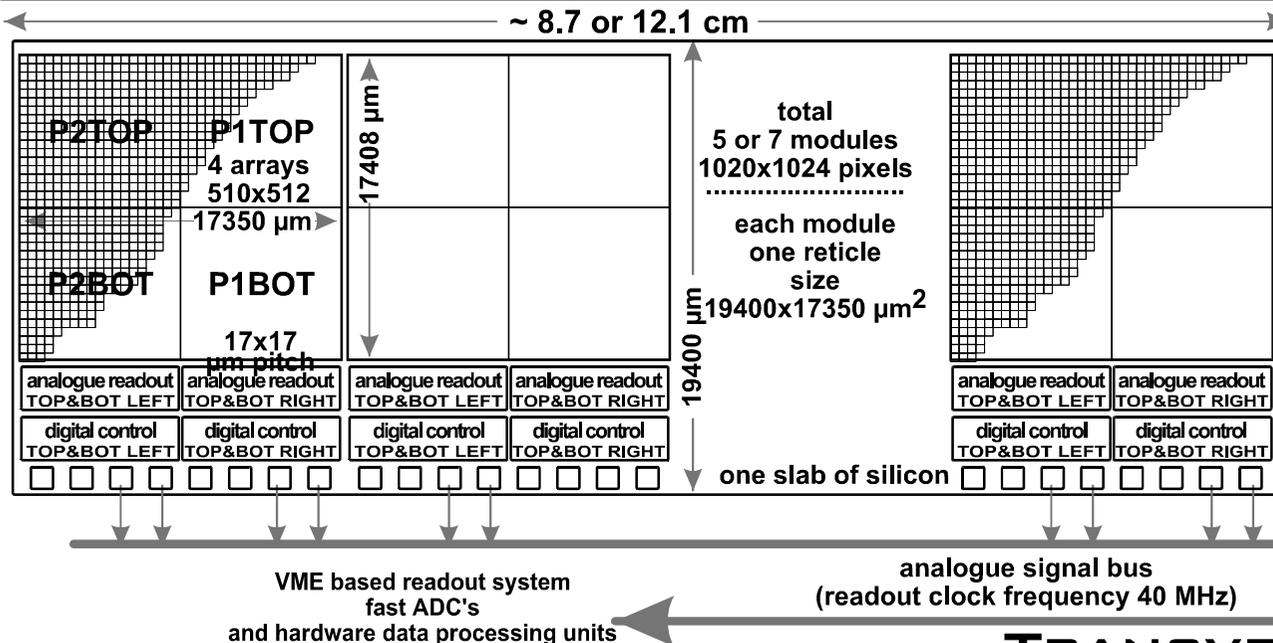


$\epsilon \sim 99\%$ ,  $S/N \sim 20-40$ ,  $\sigma \sim 1.5-2.5 \mu\text{m}$ ,  $\sigma_{2\text{hit}} \sim 30 \mu\text{m} @ 20 \times 20 \mu\text{m}^2$

The first prototypes, made of small arrays of a few thousands of pixels, demonstrated the viability of the technology and its high tracking performances. As a natural consequence, the first real scale prototype was fabricated and now tested. Following, the attention is focussed on readout strategies adapted to specific experimental conditions.



# WHERE MAPS ARE, AND PLANS FOR USE AT VX

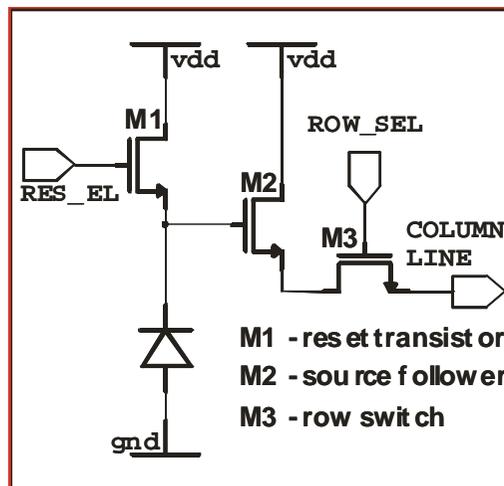


## TRANSVERSE LADDER READOUT

- ▶▶ 0.6 μm CMOS process with 14 μm epitaxial layer,
- ▶▶ 4 matrices of 510 × 512 pixels read-out in parallel; pixel: 17 × 17 μm<sup>2</sup>, diodes: P1 - 9.6 μm<sup>2</sup>, P2 - 24.0 μm<sup>2</sup>, control logic and all pads aligned along one side,

### MIMOSA V

classical  
3T  
pixel schematics

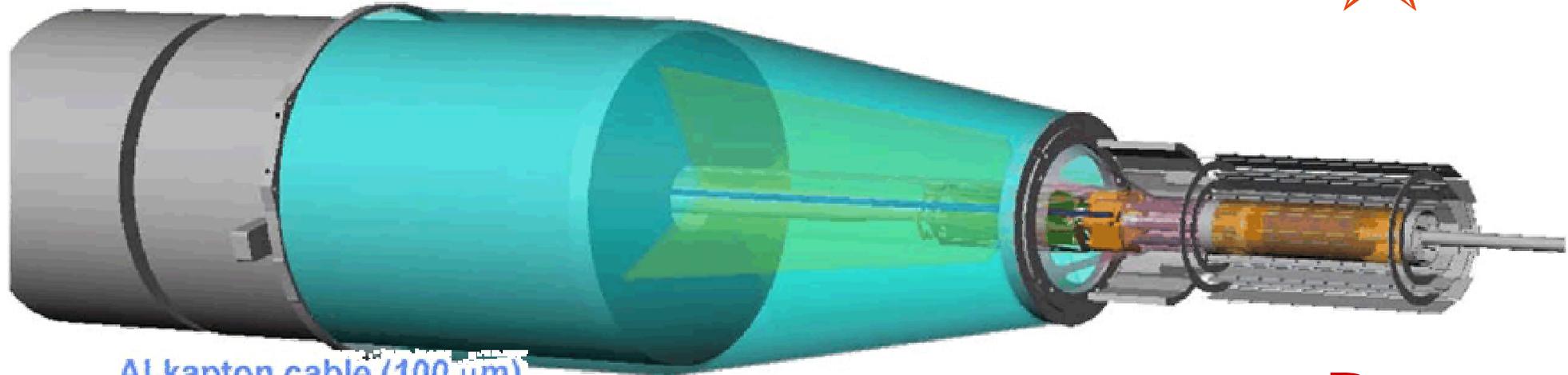


### RESULTS:

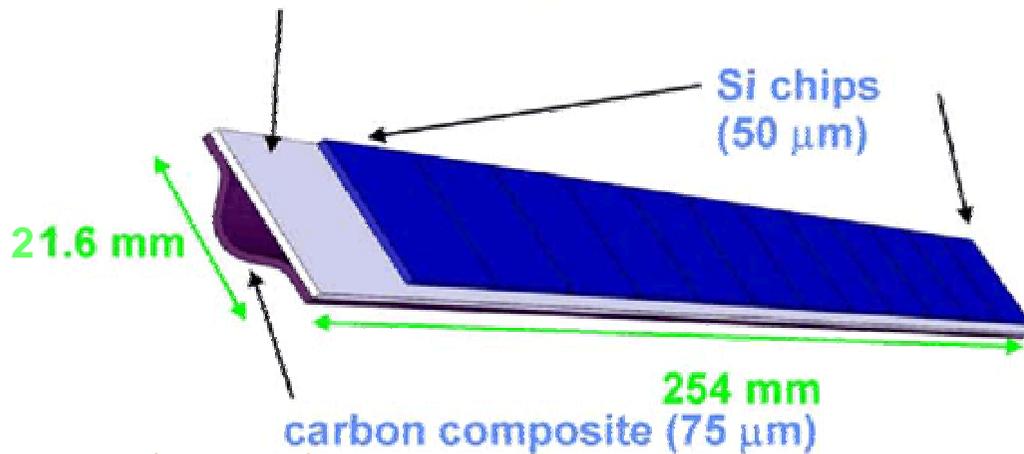
Noise mean ENC:	20.74 e <sup>-</sup>
Single pixel S/N mean:	22.73
detection efficiency ε:	99.3%
spatial resolution s:	1.7 μm
pixel-pixel gain nonuniformity	~3%
macro-scale gain nonuniformity:	~0.2%



# WHERE MAPS ARE, AND PLANS FOR USE AT VX



Al kapton cable (100  $\mu\text{m}$ )

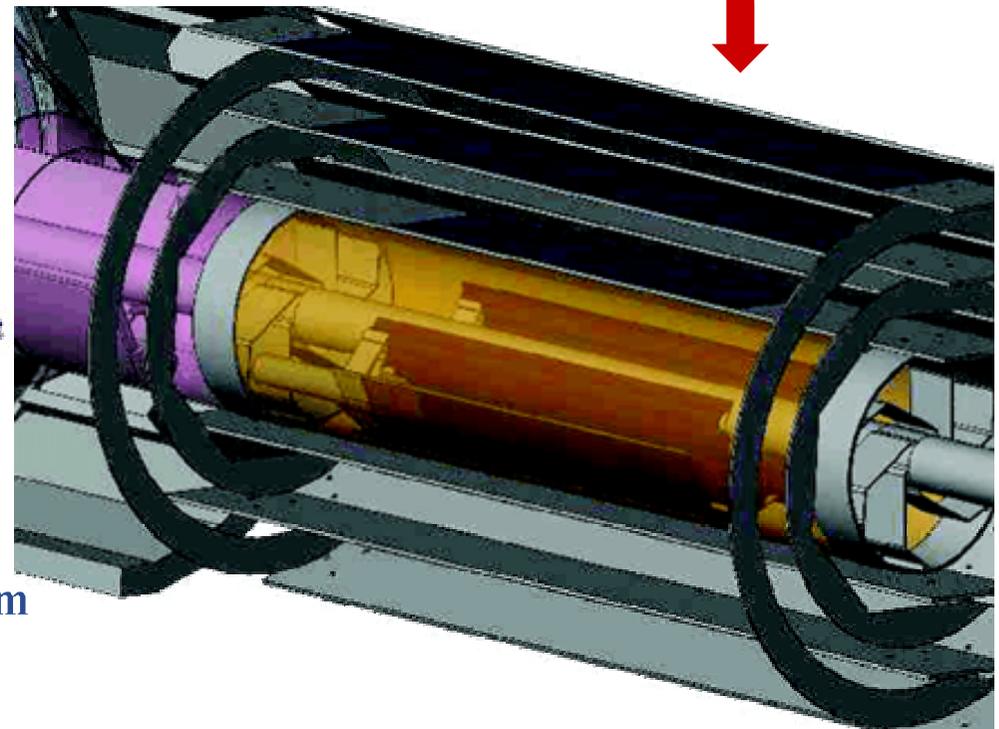


21.6 mm

254 mm

carbon composite (75  $\mu\text{m}$ )

Si chips (50  $\mu\text{m}$ )



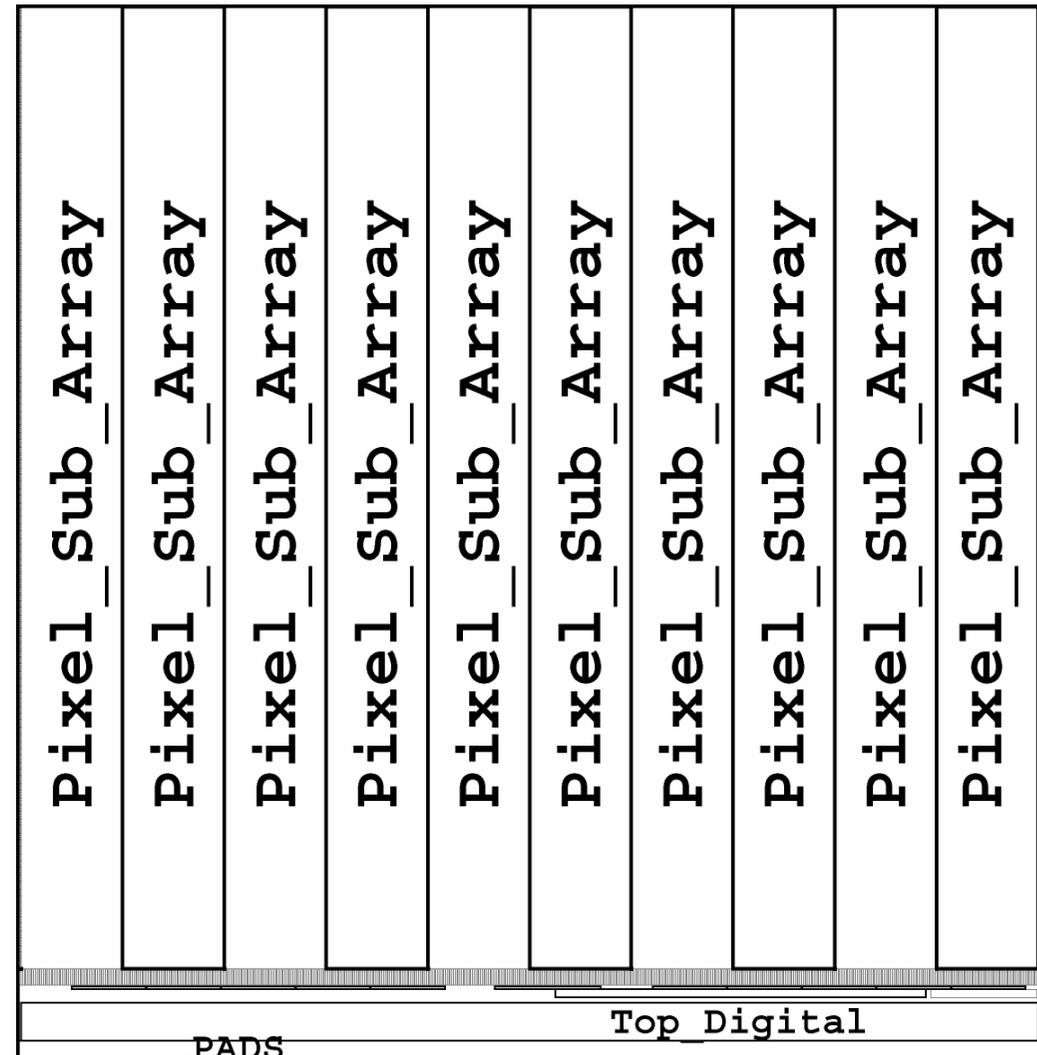
## Design details and requirements:

small radius and thin: 2 pixel layers  $\sim 1000 \text{ cm}^2$ ,  
25 ladders,  $\sim 100 \times 10^3$  pixels,  $R_{L1} \sim 1.5 \text{ cm}$ ,  $R_{L2} \sim 4 \text{ cm}$   
silicon thickness  $\sim 50 \mu\text{m}$ , pitch  $20 \times 20 \mu\text{m}^2 - 30 \times 30 \mu\text{m}^2$   
readout speed 10-20 ms thus 50 Hz – 100 Hz



## ▶▶ MIMOSA - STAR CHIP

- ▶▶ subdivision in 10 groups of  $64 \times 64$  pixels read-out in parallel with multiplexed outputs,
- ▶▶ each group splitted in 2 sub-groups of 32 columns (*to gain in speed*),
- ▶▶ active area:  $19.2 \times 19.2 \text{ mm}^2$ , readout part:  $1.5\text{-}1.7 \times 19.2 \text{ mm}^2$ , chip dimensions:  $19.2 \times 19.2 \text{ mm}^2$ ,
- ▶▶ clocks: pixel level - *slow (power + noise)*; chip processing level - *fast (small total integration time <5ms)*,
- ▶▶ continuous frame analogue readout option: single fast (*100 MHz multiplexed output*) or 10 slow parallel outputs,
- ▶▶ JTAG remote control (*bias + tests*).



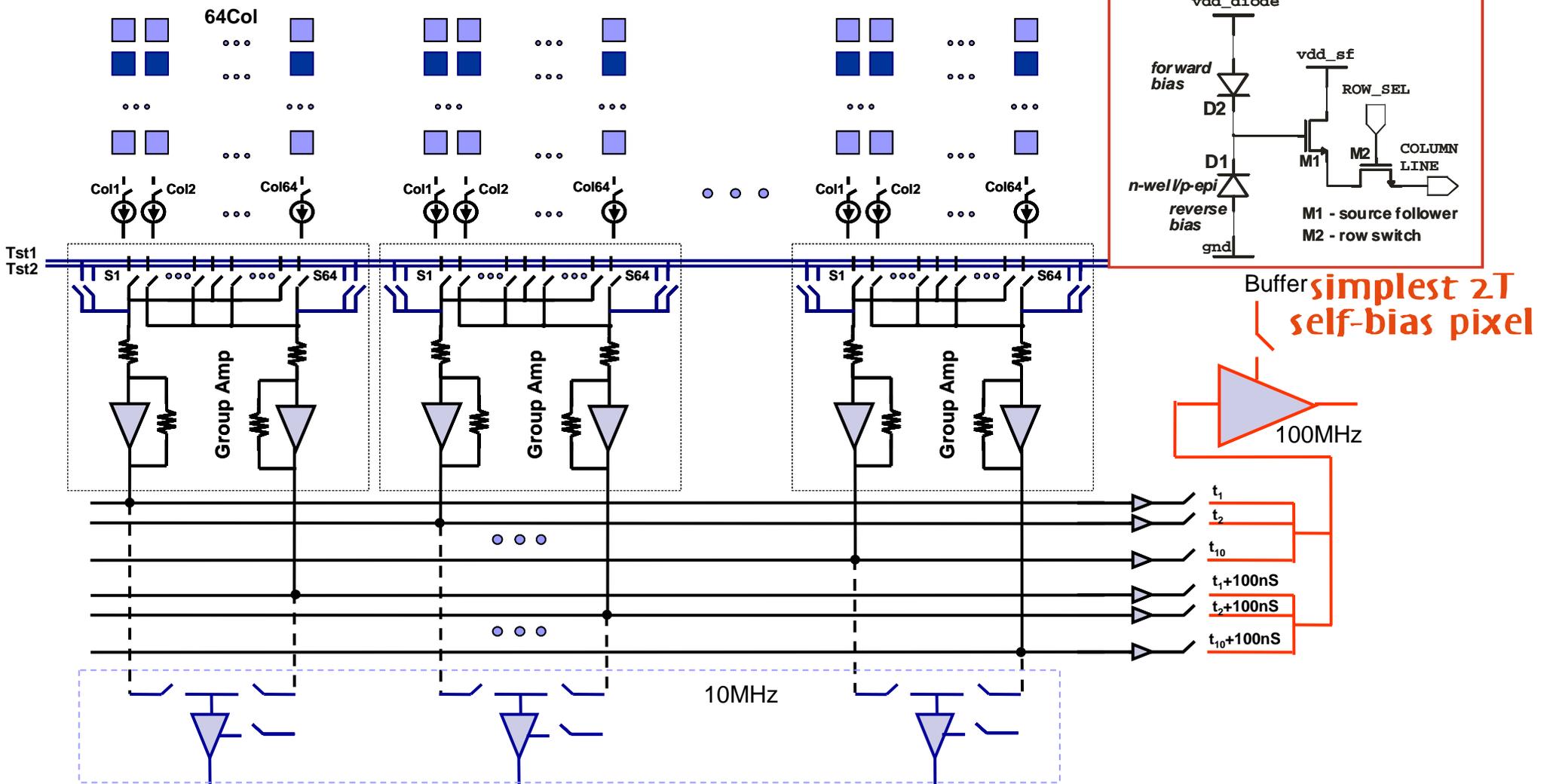
CHIP UNDER DEVELOPMENT - SUBMISSION OF  
SMALL PROTOTYPE ( $2 \times 64 \times 128$ ) IN TSMC  
 $0.25 \mu\text{m}$  ( $8 \mu\text{m}$  EPI-LAYER) IN JULY 2004



WHERE MAPS ARE, AND PLANS FOR USE AT VX



MIMOSA - STAR CHIP ARCHITECTURE



NEW STAR VXD IS AN INTERESTING AND IMPORTANT EXPERIENCE FOR BOTH MAPS TECHNOLOGY AND ENGINEERED DETECTOR DESIGN.

**HOW FAR TO FULFIL FLC REQUIREMENTS (☢,  $\sigma$ , 📊 ...)**

**RADIATION HARDNESS**

$$\frac{1}{\tau_R} = \frac{1}{\tau_0} + \kappa_{\tau} \Phi$$

**▶▶ NEUTRON IRRADIATIONS**

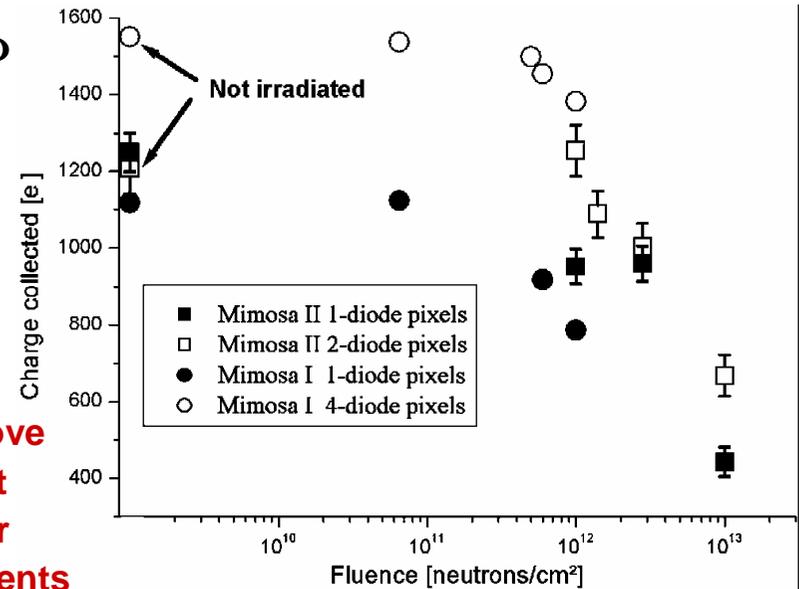
tests up to  $10^{13} n_{1\text{MeVeq}}/\text{cm}^2$

fluences up to  $10^{12} n_{1\text{MeVeq}}/\text{cm}^2$  are still acceptable (2 orders of magnitude above FLC requirements =  $10^9 n_{1\text{MeVeq}}/\text{cm}^2/\text{year}$ )

**▶▶ IONISING IRRADIATIONS**

tests up to a few 100 krad

doses up to this level acceptable above FLC requirements 50 krad/year, exact sources of performance losses under investigation (diode size and placements of transistors are important parameters)



**$\sigma$  TRACKING PERFORMANCES**

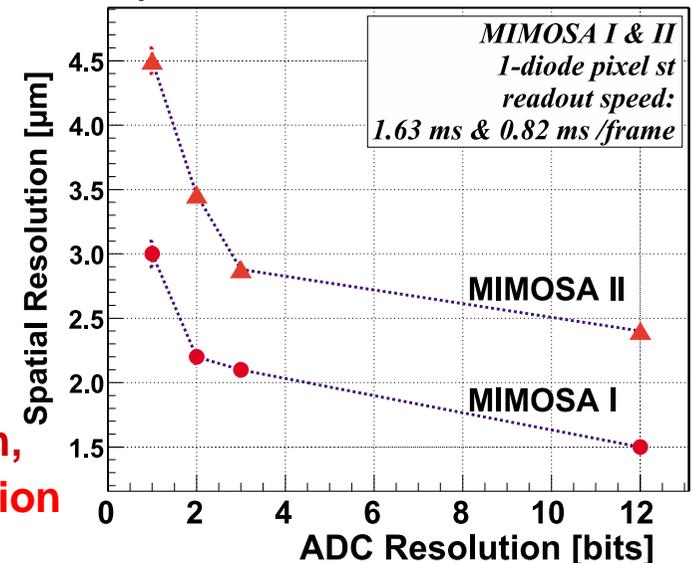
**▶▶ IMPACT POINT SPATIAL RESOLUTION**

$\sigma_{sp} = 2-2.5 \mu\text{m}$  for 3 bits encoding,  $\epsilon_{tr}$  close to 100%, double hits distinguishable down to 30  $\mu\text{m}$  distance.

**▶▶ MATERIAL BUDGET**

the goal of  $X/X_0 \sim 0.1\%$ /layer achievable in thinning to 50  $\mu\text{m}$ , recent achievement: thinning to 15  $\mu\text{m}$  for backside exposition for low energy  $\beta$  detection.

**Spatial Resolution vs ADC Resolution**





# HOW FAR TO FULFIL FLC REQUIREMENTS (☢, $\sigma$ , ⚡ ...)

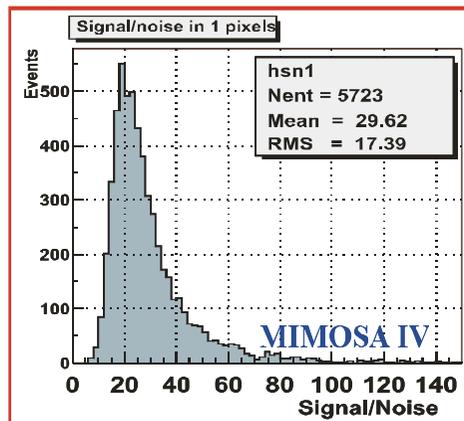
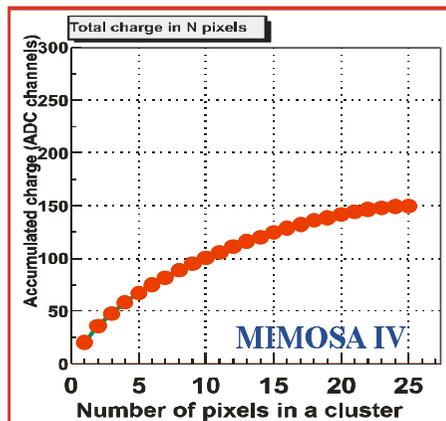
## MIMOSA TECHNOLOGY OPTIONS

▶ Original MAPS implementations use the epitaxial layer as a sensitive volume. Alternatively, non-epitaxial, intrinsically lightly doped substrates, typical for RF CMOS, can also be used.

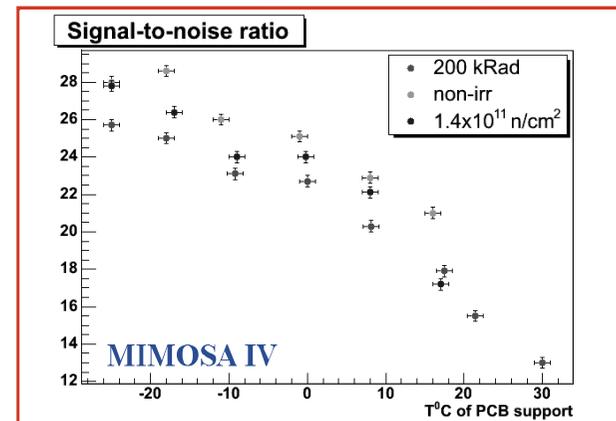
**MIMOSA IV no epi (summary): SUCCESSOR II no epi (summary):**

SB design  $\epsilon \sim 99.5\%$ ,  $\sigma \sim 2.5 \mu\text{m}$ , @  $20 \times 20 \mu\text{m}^2$

SB design  $\epsilon \sim 99.9\%$ ,  $\sigma \sim 5-6 \mu\text{m}$  (larger diodes) @  $40 \times 40 \mu\text{m}^2$



$\tau_e$  and  $\mu_e$  depend strongly on temperature affecting charge collection in the sensor



▶ Expanding market of commercial visible light imagers entails equal development of dedicated fabrication processes. Those become available for wide public - MIMOSA IX submitted for fabrication using such a dedicated process...

- mixed-signal polycide gate CMOS, 4 metal, 2 poly, high-resistive poly, 3.3V and 5V gates,
- optimized N-well diode leakage current  $< 45 \text{ pA/mm}^2$  @  $27 \text{ }^\circ\text{C}$  - according to foundry documentation,
- $\sim 20 \mu\text{m}$  epitaxial lightly doped substrate, (samples on non-epi high resistivity substrate also available),
- availability in multiproject submissions in 2004 - reasonable pricing.

HOW FAR TO FULFIL FLC REQUIREMENTS (,  $\sigma$ ,  ...)

## READOUT SPEED

## ▶ DETERMINATION OF THE READOUT SPEED

▶ Beamstrahlung (*TESLA*):

according to simulations one may expect:

$$N|_{90^\circ} \approx 5e^{\pm}/\text{cm}^2/\text{BX} @ 500 \text{ GeV and } R_{L1} = 15\text{mm}$$

deducing occupancy one finds  $\approx 3\text{-}5\%$  in  $100 \mu\text{s}$  ( $m_{\text{clust}} \approx 5$ )

$$t_{L1-L2} \approx 25\text{-}50 \mu\text{s} \text{ (R\&D running)}$$

$$t_{L3-L5} \approx 100 \text{ up to } 200 \mu\text{s} \text{ (achievable with current state of MAPS development)}$$

▶ Machine time structure *cold and warm LC*

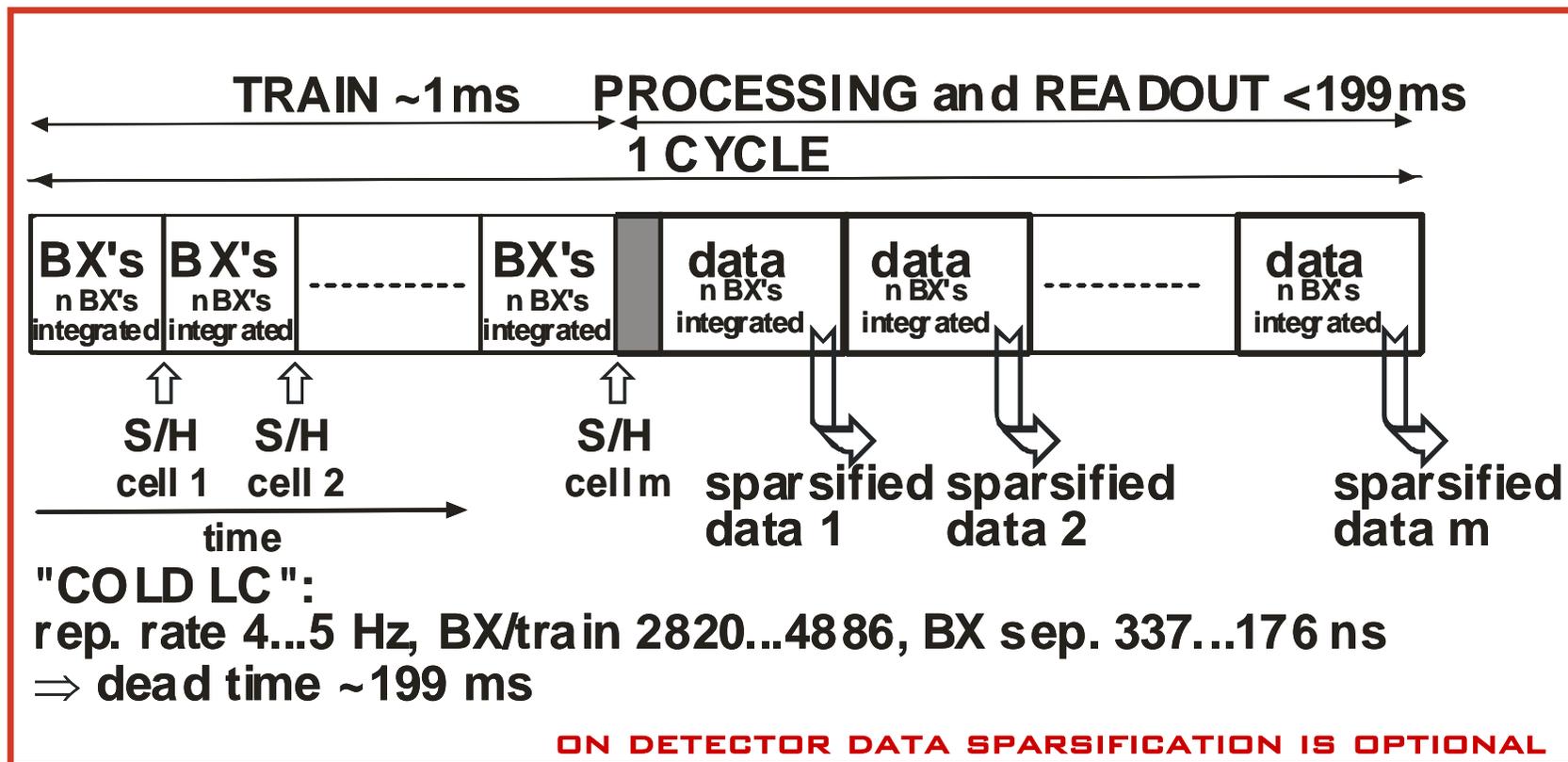
- L3-L5  multiple readout during beam-on (*train*) interval with on-line signal processing and result data transfer,  
 multiple sampling of signals during beam-on (*train*) time onto on-pixel capacitors and readout in between trains.
- L1-L2  fast, column || on line data processing with hit/cluster selection.

warm LC  integration over single train and data transfer in between trains, possible data processing with hit/cluster selection for data reduction.



**RDOUT STRATEGIES FOR WARM & COLD FLC**

▶▶ **READOUT OF L3-L5 FOR COLD LC**



• Multiple scans of the whole detector with sampling data on pixel at the required speed (~200 μs) during the beam-on interval and then read the samples out when the beam is off.

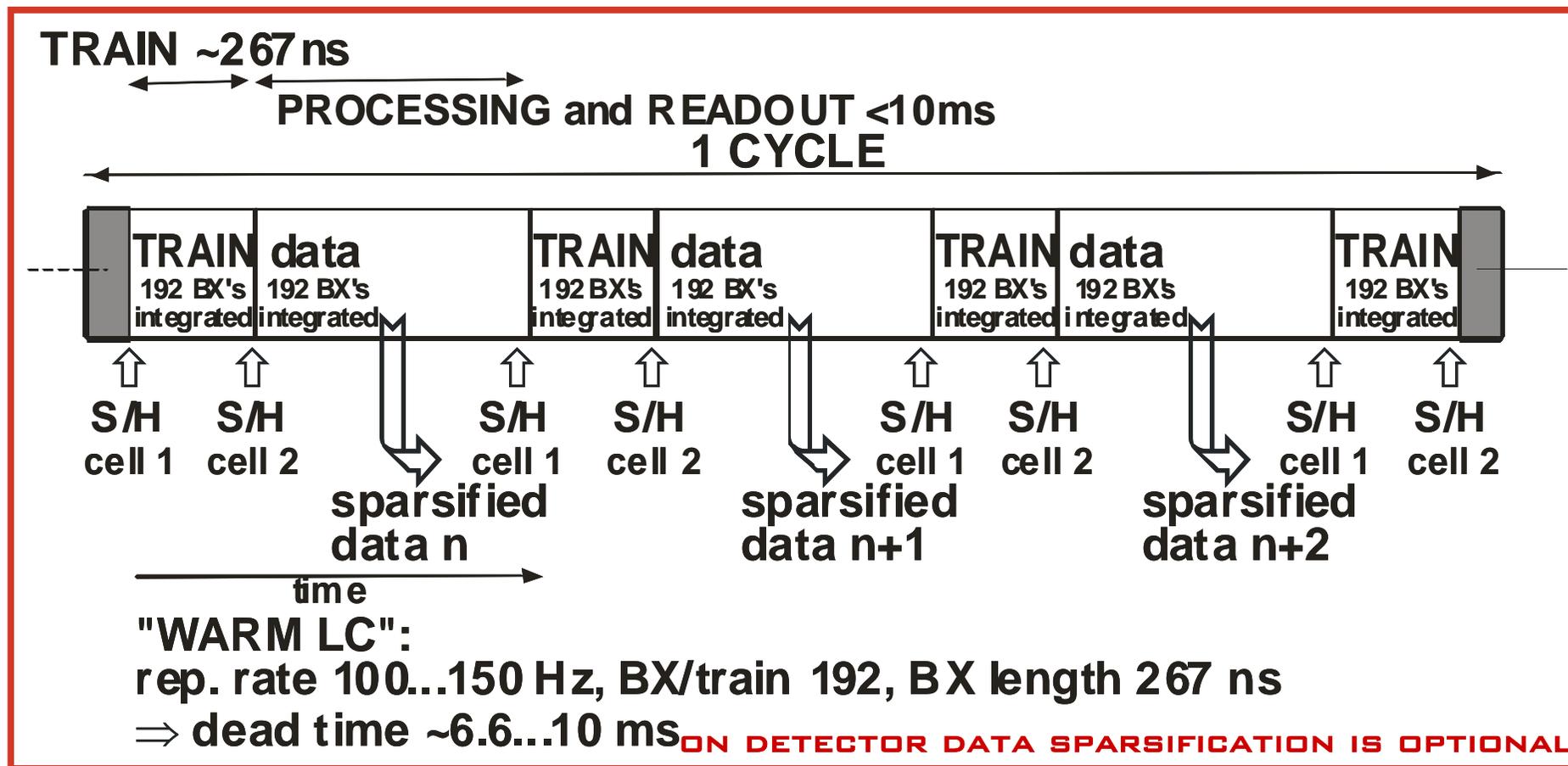
▶▶ FOR L1 & L2 DEVELOPMENT OF FAST PARALLELY PROCESSING μCIRCUITS IS NECESSARY !  
OR MORE CELLS AND FASTER SCAN?





# READOUT STRATEGIES FOR WARM & COLD FLC

## ▶ READOUT FOR WARM LC

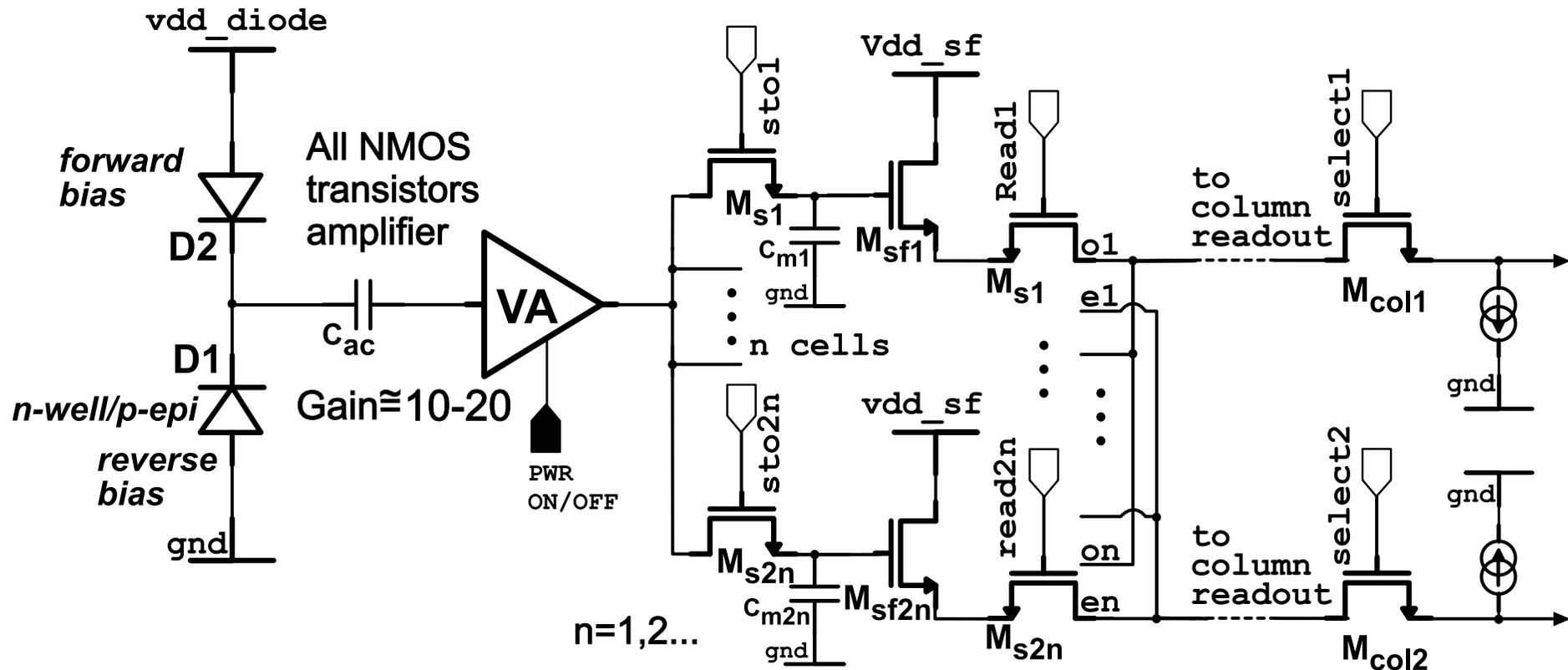


- only two on pixel memory cells (for beginning and end of integration levels) are required, can be fitted with pixel designs MIMOSA VI, VII, VIII and IX,
- integration over 192 BX within one train,



# RDOUT STRATEGIES FOR WARM & COLD FLC

## ▶ READOUT OF L3-L5 FOR COLD LC



- use of auto reverse bias system fo charge collecting diode,
- only NMOST AC-coupled amplifier,
- coupling of each memory cell to separate SF transistor, charge division ↘ and no gain losing.



# DEVELOPMENT OF FAST RDOUT CIRCUITS

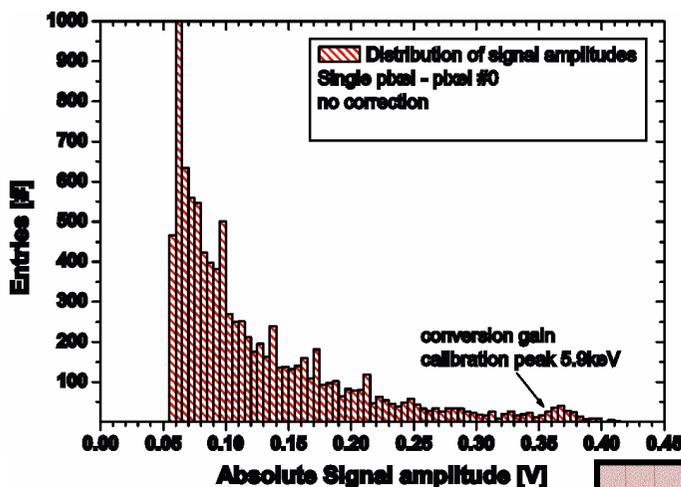
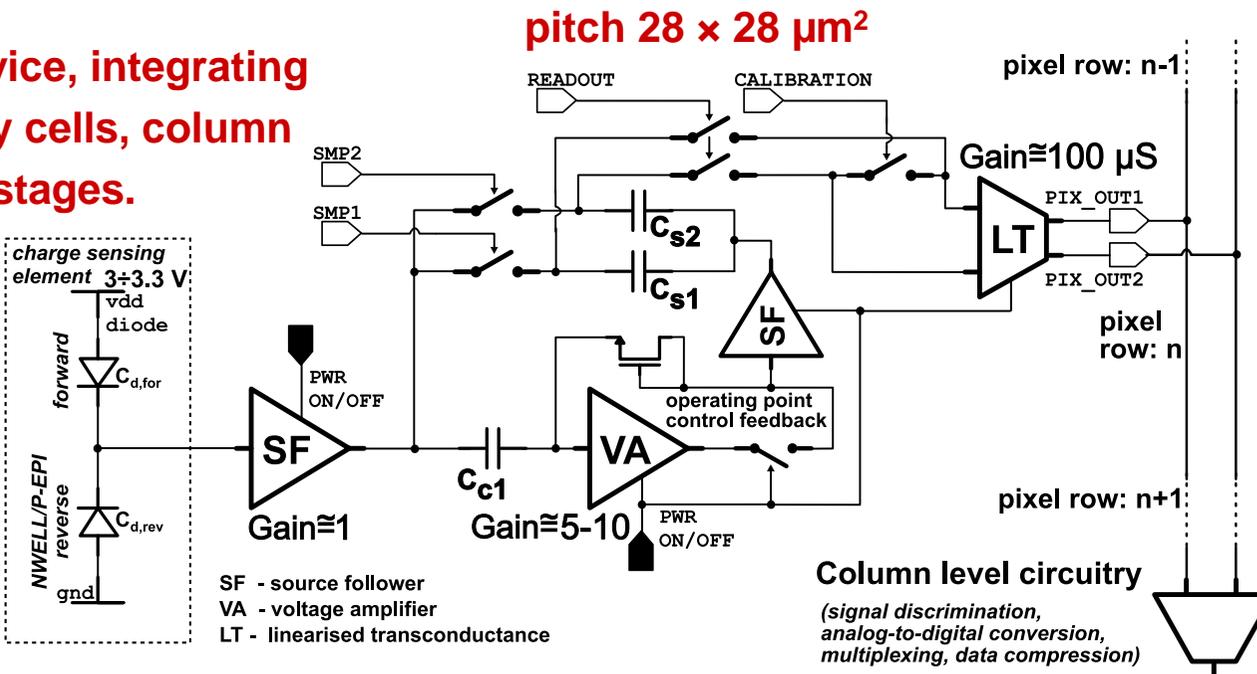
## ▶▶ MIMOSA VI

▶▶ MIMOSA VI - first tested device, integrating on-pixel voltage mode memory cells, column || readout, and discrimination stages.

▶▶ main features:

- mixed 0.35  $\mu\text{m}$  process with 4  $\mu\text{m}$  epitaxial layer,
- array of 128 rows  $\times$  30 columns read in || with CDS +signal discrimination (total 25  $\mu\text{s}$ )
- AC coupled on-pixel voltage amplifier + CDS,
- conversion gain  $\sim 6.5 \text{ nA/e}^-$ ,

pixel + basic processing needs power typically  $3\text{-}5 \times 100 \mu\text{W}$  /col./rd cycle



## MIMOSA VI pixel and discriminator tests summary

MIMOSA VI				features		
performances of chip designed				noise ENC: $\sim 20 \text{ e}^-$ , conversion gain: $6.5 \text{ nA/e}^-$ pixel dispersions: $\sim 120 \text{ e}^-$		
discriminator performances						
$\tau_1 \text{ ns}$	$\tau_2 \text{ ns}$	$\tau_3 \text{ ns}$	$\tau_4 \text{ ns}$	noise inp.ref.	offset inp.ref.	power
90	15	45	30	$\sim 85 \mu\text{V}_{\text{rms}}$	negligible	$\sim 200 \mu\text{W}$
75	12.5	62.5	25	$\sim 100 \mu\text{V}_{\text{rms}}$	$\sim 400 \mu\text{V}$	$\sim 200 \mu\text{W}$
60	15	45	30	$\sim 100 \mu\text{V}_{\text{rms}}$	$\sim 900 \mu\text{V}$	$\sim 200 \mu\text{W}$

MVI DESIGNED IN COLL. WITH CEA/DAPNIA.



# DEVELOPMENT OF FAST RDOUT CIRCUITS

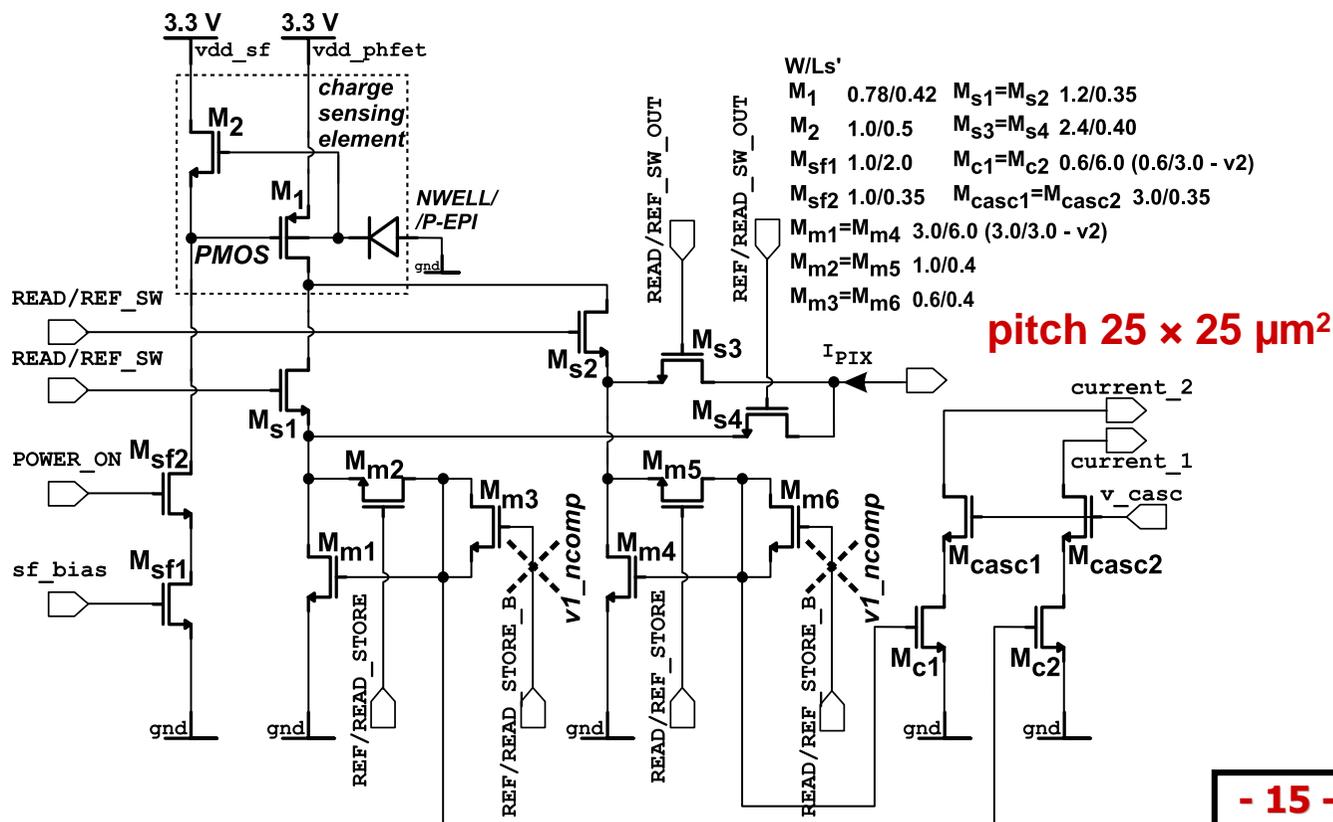
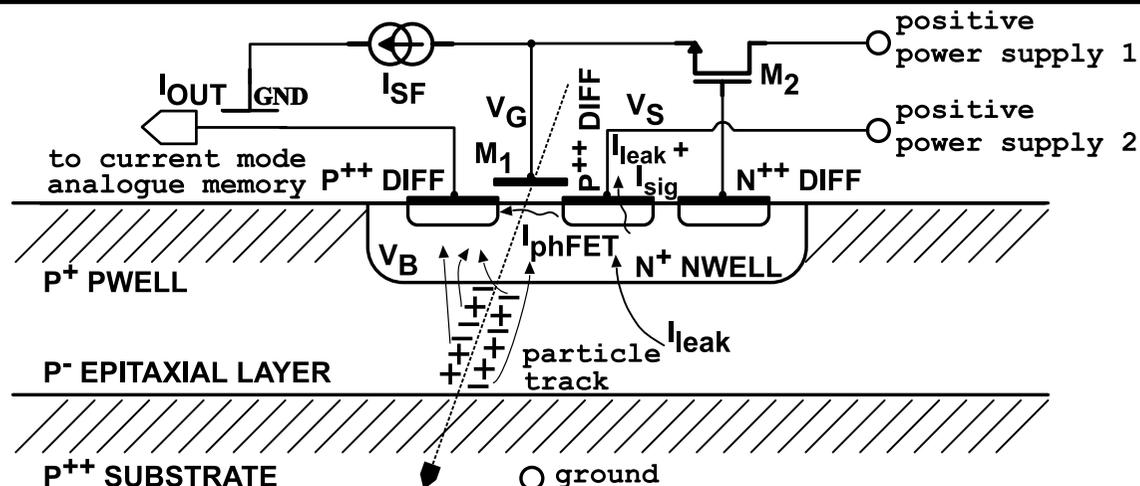
## ▶▶ MIMOSA VII

### ▶▶ MIMOSA VII - MAPS device

integrating pixel with charge sensitive element similar to DEPFET, but all processing electronics integrated on the same circuit!

#### ▶▶ main features:

- mixed 0.35  $\mu\text{m}$  process w/o epitaxial layer,
- array of 64 rows  $\times$  16 columns read in || with CDS (total 20  $\mu\text{s}$ )
- photoFET CSE,
- conversion gain  $\sim 500 \text{ pA/e}^-$ ,



photoFET possibility of ganging outputs for preselection of zones for readout

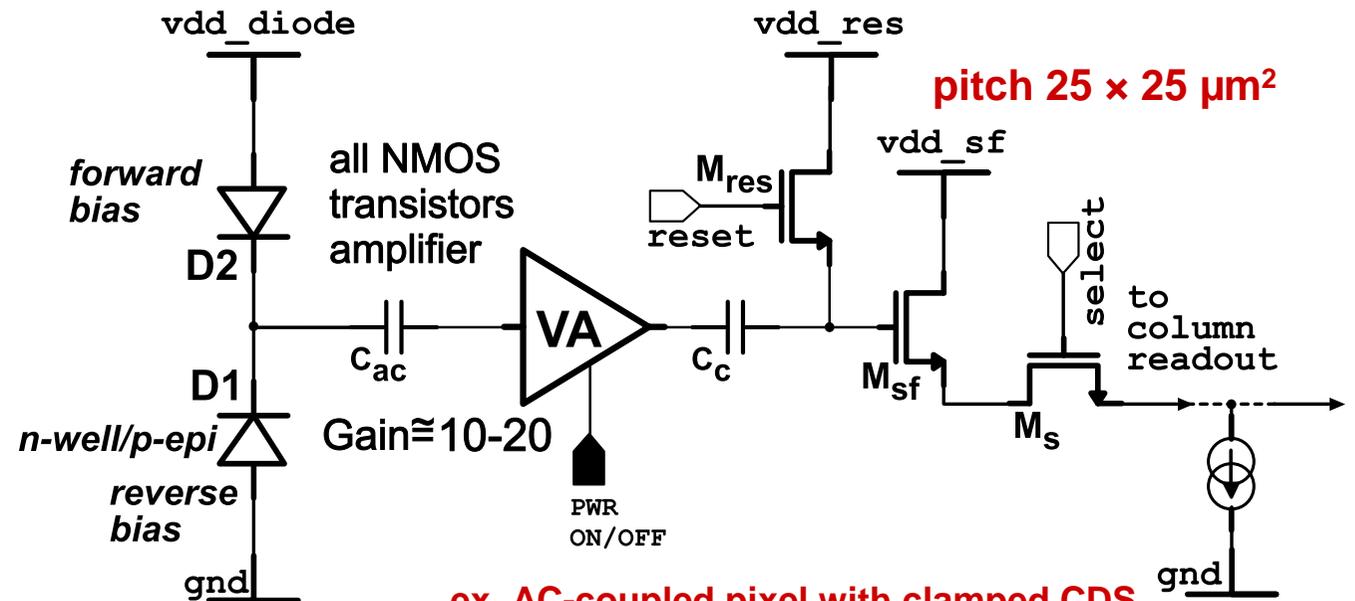
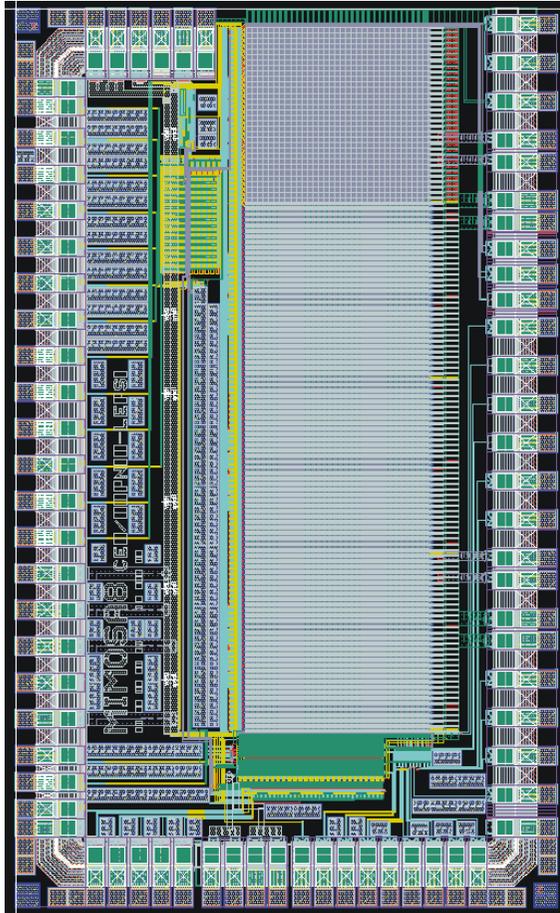
TESTS UNDER PREPARATION.





# DEVELOPMENT OF FAST READOUT CIRCUITS

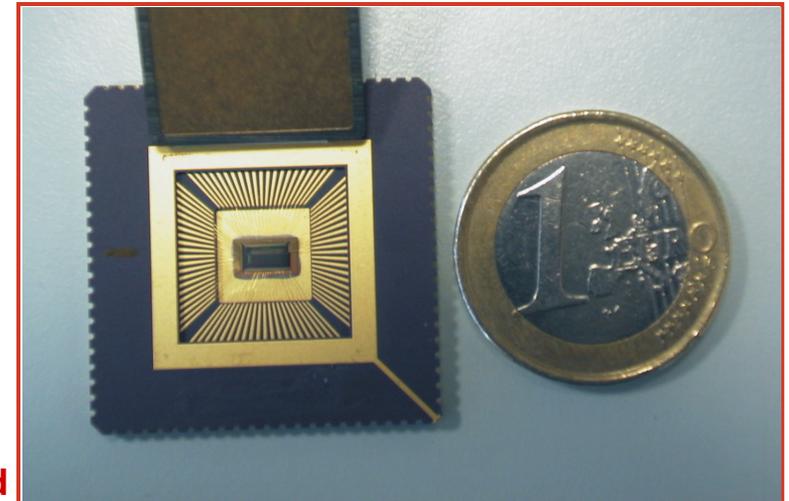
## ▶ MIMOSA VIII



ex. AC-coupled pixel with clamped CDS

▶ main features:

- digital 0.25  $\mu\text{m}$  process with 8  $\mu\text{m}$  epitaxial layer,
- array of 128 rows  $\times$  32 columns read in || with CDS + signal discrimination (total 20  $\mu\text{s}$ )
- only NMOS transistors + n-well/p-epi diodes,
- DC and AC coupled on-pixel voltage amplifiers + CDS,
- conversion gain 30-60  $\mu\text{V}/\text{e}^-$  and 150  $\mu\text{V}/\text{e}^-$ ,



TESTS UNDER PREPARATION.



MVIII DESIGNED IN COLL. WITH CEA/DAPNIA.



## CONCLUSIONS + FUTURE R&D

- ▶ MAPS TECHNOLOGY PROVED FOR HIGH PERFORMANCE CHARGED PARTICLE TRACKING,
- ▶ MAPS KNOW-HOW CLOSE TO SATISFY **WARM** LC,  
... AND FOR EXTERNAL LAYERS OF **COLD** LC,
- ▶ STAR VXD PIONEERING THE USE OF MAPS,
- ▶ TESTS OF THE SECOND GENERATION DETECTORS M6/M7/M8/M9 WILL HELP TO CHOOSE WORKING-HORSE FOR FUTURE DEVELOPMENT - INCLUDING FAST AND INTELLIGENT DETECTOR (*MORE ADVANCED PIXEL ARCH. THAN CLASS. 3T*),
- ▶ R&D NECESSARY FOR L1 & L2 OF **COLD** LC (*PROTOTYPING AND TESTING - BUT THERE ARE CANDIDATES*),
- ▶ OTHER EXPERIMENTS E.G. CBM @ GSI (*RAD. HARDNESS + READOUT SPEED MORE AGGRESSIVE*) ARE JOINING,
- ▶ BE PREPARED TO FACE SURPRISES, E.G. BEAM PICK-UP NOISE, ETC.