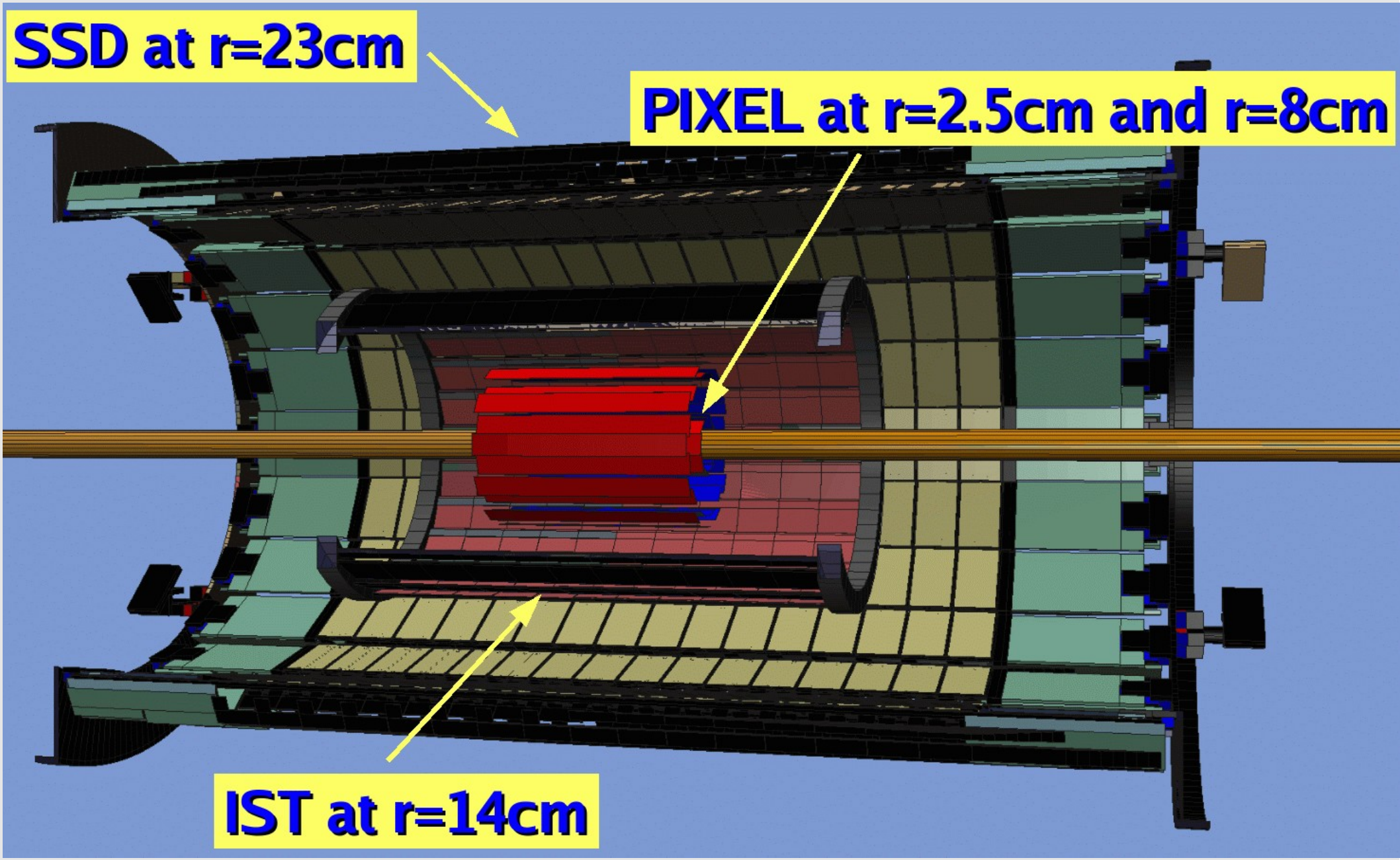
IST mechanics

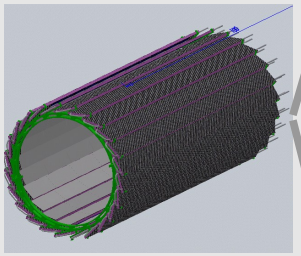
IST in HFT

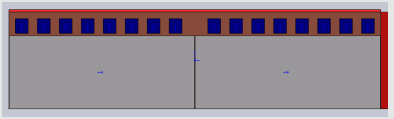


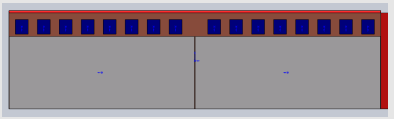
IST requirements

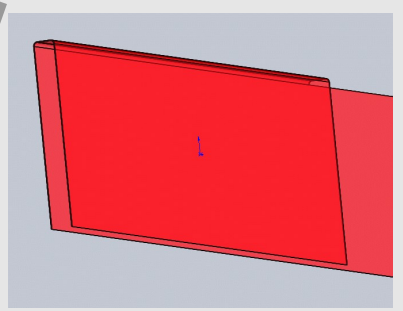
- **Location**: Between PIXEL and SSD covering $-1 < \eta < +1$
- **Material budget**: <1.5% X0 per layer ($-1 < \eta < 1$) and <10% X0 ($1 < \eta < 2$)
- **Occupancy**: <10% for central Au+Au events at 200GeV
- **Tracking efficiency / purity**: Meet physics requirements for efficient D0 reconstruction
- **Rate capability**: Handle RHICII peak luminosities for Au+Au and p+p
- **Sampling speed**: Resolve individual beam bunches (107ns - bunch crossing time)

The IST tree

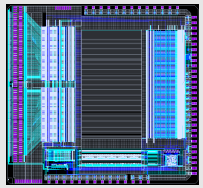




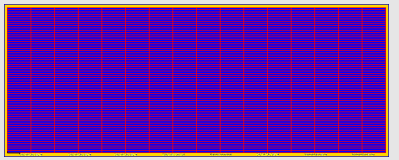




72 hybrids



1152 chips

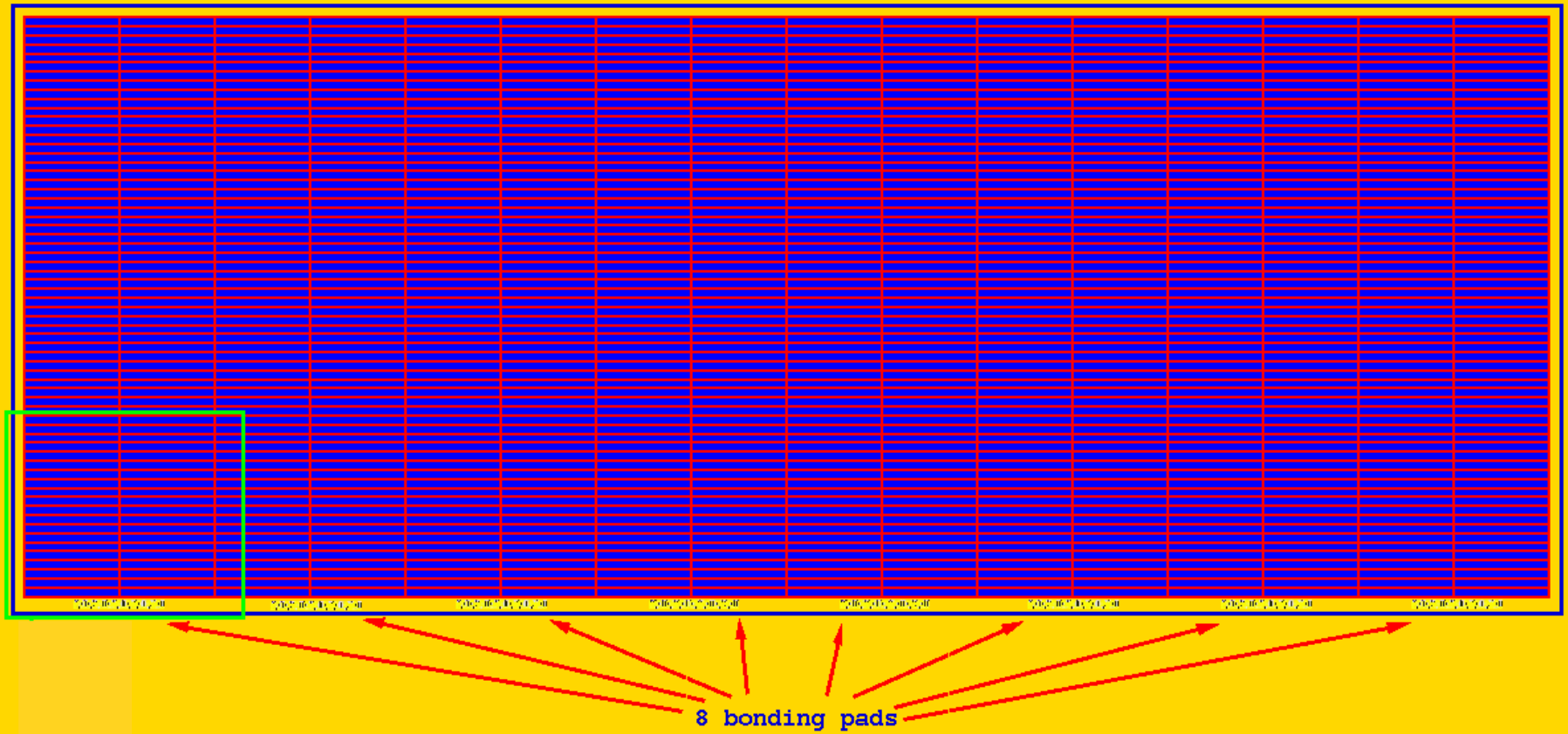


24 ladders

72 modules

144 sensors

Silicon pad sensors



Quotation came in on budget
Very close to final design, which will be shorter

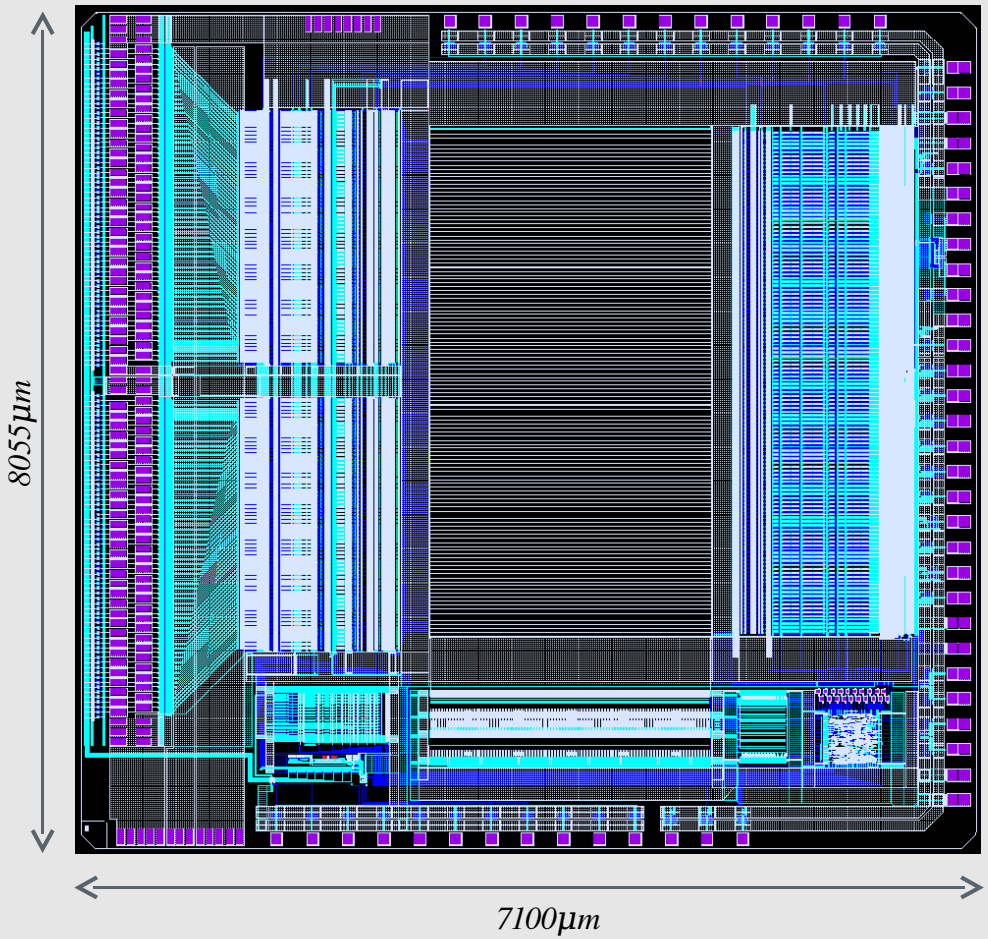
Occupancy: 2%
(for Au+Au @ 200GeV)

Silicon sensor size (cut edge): 102mm x 40mm
Active area pitch (grid size): 6275um x 596um in 16 columns x 64 rows
Distance cut edge to active area left & right: 800um
Distance cut edge to active area top: 800um
Distance cut edge to active area bottom: 1056um

Metal-2 signal traces not shown in this design!

HamamatsuDesign_17Jun2008 I
Latest Revision: 06/25/2008
Scale:

APV25-S1 readout chip

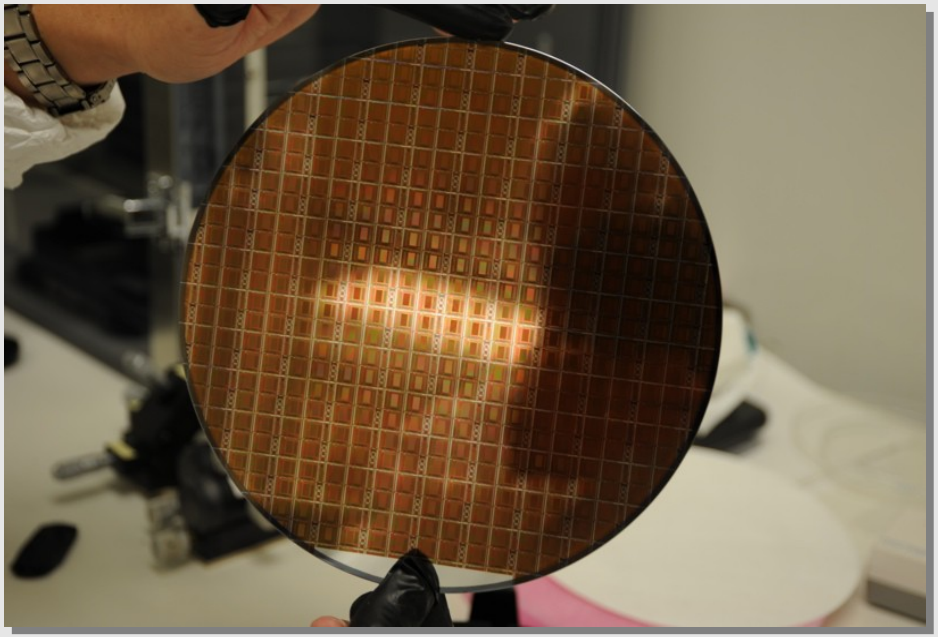


- Developed for CMS (75000 in CMS tracker) and also used by COMPASS for triple-GEM detector readout
- 0.25µm CMOS
- 128 channels
- 40 MHz sampling rate
- 4µs analogue pipeline
- 11:1 Signal / Noise
- 0.30 Watt/chip
- Radiation hard

Handles RHICII peak luminosities for Au+Au and p+p

Resolves individual RHIC beam bunches (107ns)

APV25-S1 procurement

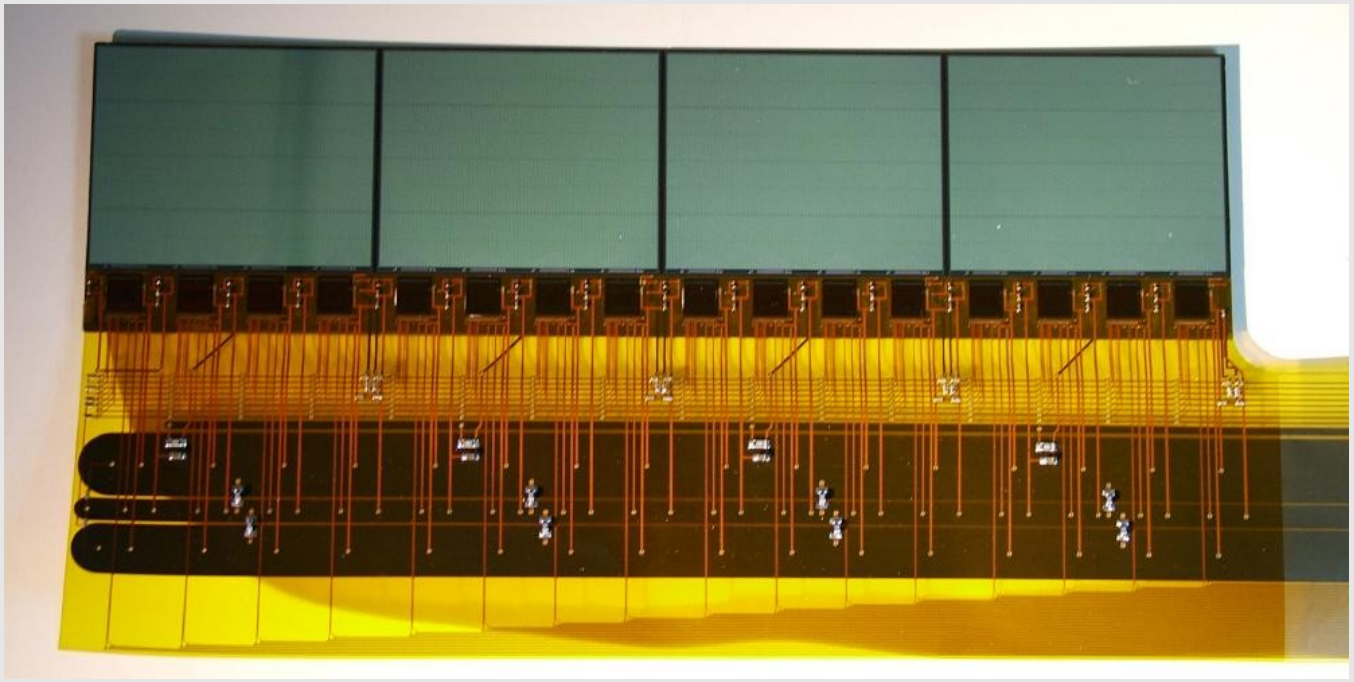


8 wafers procured from CMS

Should give ~2600 good chips

1 wafer has been diced, chips are being mounted for testing before rest gets diced

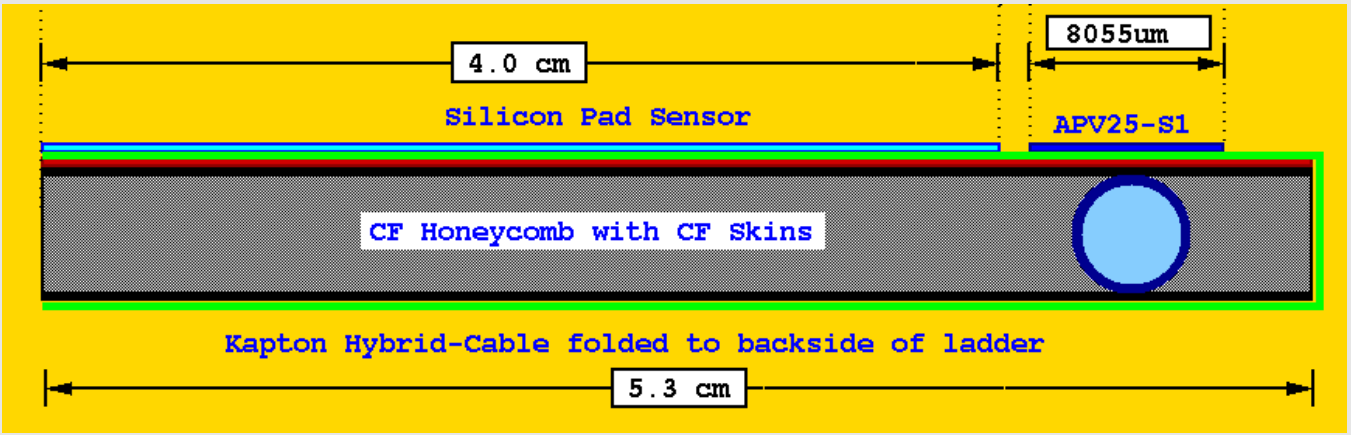
Kapton hybrid/cable



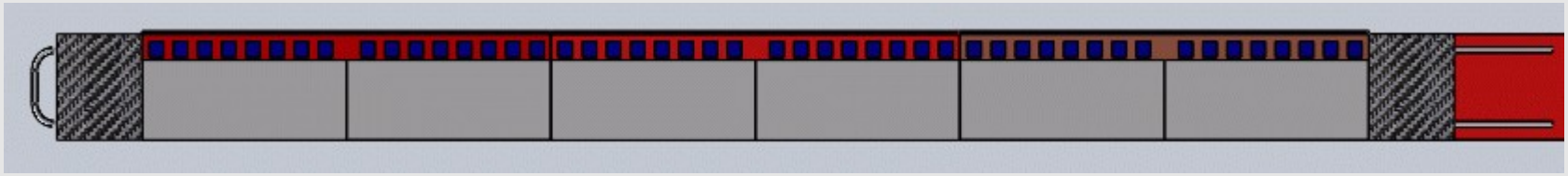
250um thick kapton (plus some Cu)

~1m cable folds over to back of ladder

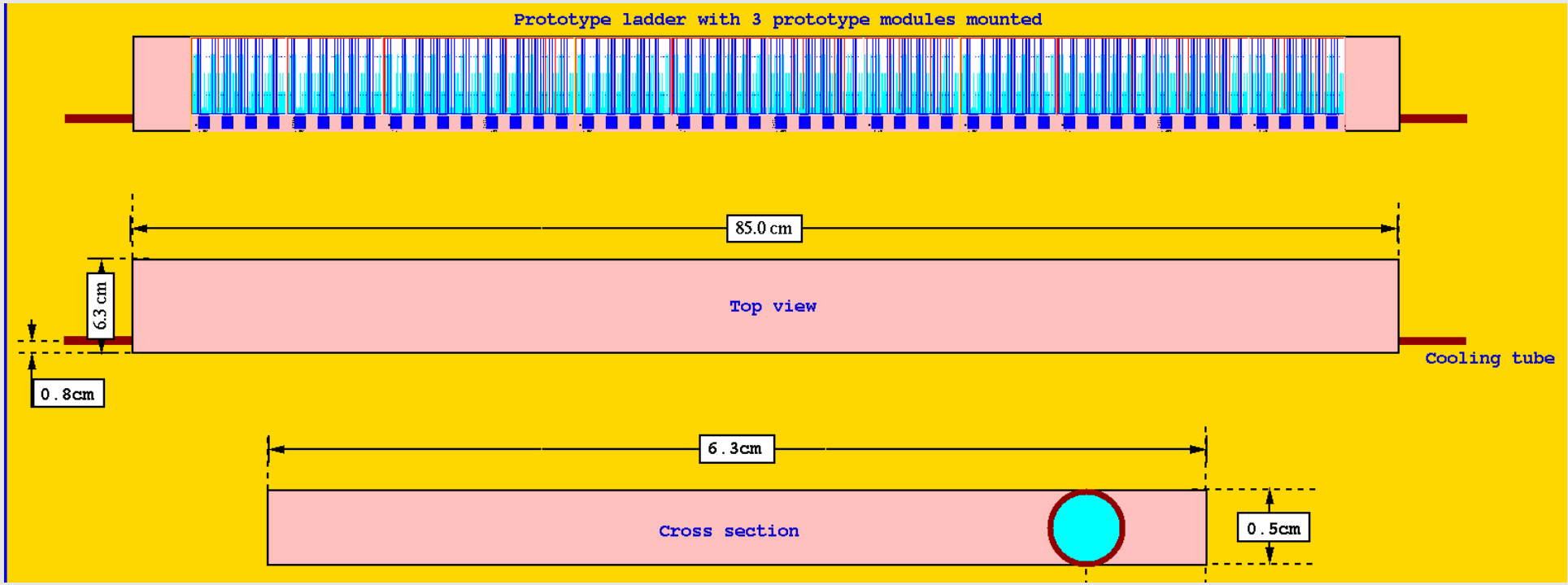
2 prototypes are being assembled



Carbon fiber honeycomb ladder



Covers -1.5 < n < +1.5, so can be shorter
= shorter sensors, less chips/dissipation, stiffer ladders



Ladder prototype

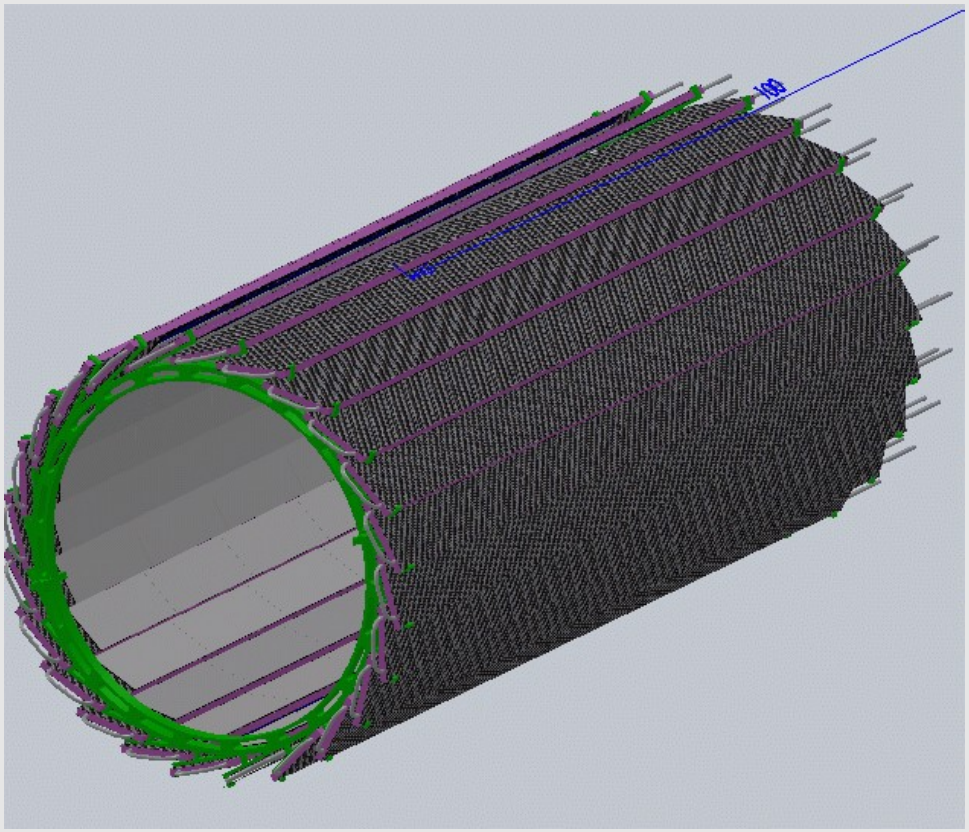
Produced at LBNL

Will be used for mechanical and cooling tests

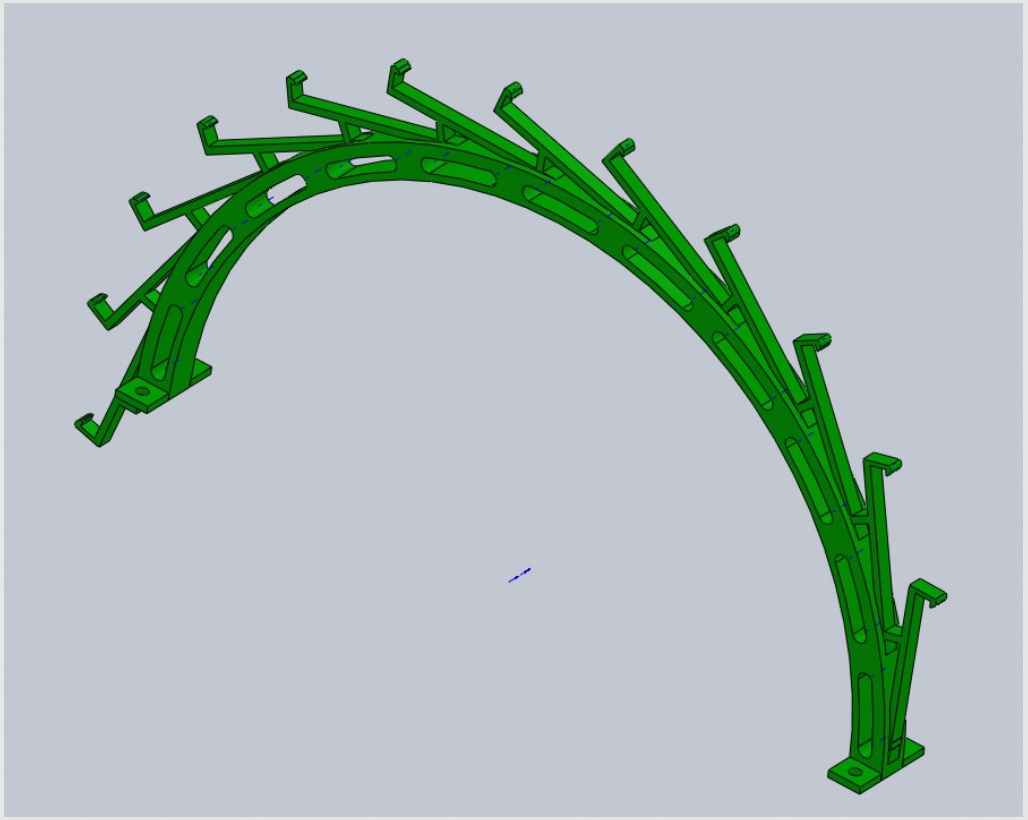
Much longer than final ladder because it has to accommodate the long prototypes

Decision on 1 or 2 cooling channels still to be made

IST barrel and support



24 IST ladders at R=14cm



Clip-on crown support

The limited size and weight of the ladders make this an 'easy' design

However, assembly and survey issues could make a sub-structure (clamshell) necessary

Integration requirements

Active element spatial error 50um to 100um

Support cylinder to attach IST support brackets

Cooling system capable of handling 400 Watt

The IST will need to feed out 72 cables with a total cross-section of ~250 cm^2 and a mass of ~20 kg/m

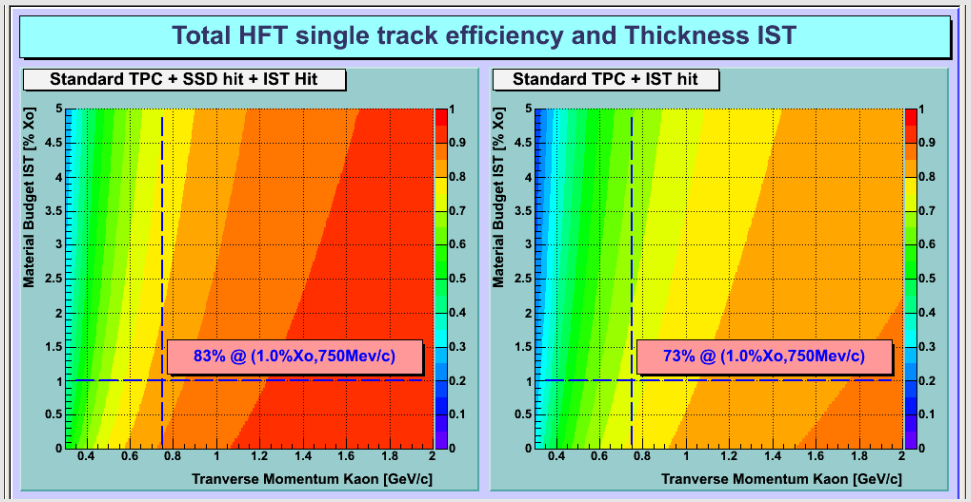
There will be 48 Aluminum cooling tubes with a total cross-section of ~160 cm^2 and a mass of ~7 kg/m

Concluding

Reasonably small conservative design

- Silicon Pad sensors similar to PHOBOS sensors
- Readout chips pioneered by CMS
- Feasible kapton hybrid/cable design
- Ladder and support structure derived from ATLAS upgrade

Current design meets all requirements so far



Final design this summer

General requirements

Active element spatial error 50um to 100um

Support cylinder to attach IST support brackets

Cooling system capable of handling 400 Watt

The IST will need to feed out 72 cables with a total cross-section of ~250 cm^2 and a mass of ~20 kg/m

There will be 48 Aluminum cooling tubes with a total cross-section of ~160 cm^2 and a mass of ~7 kg/m