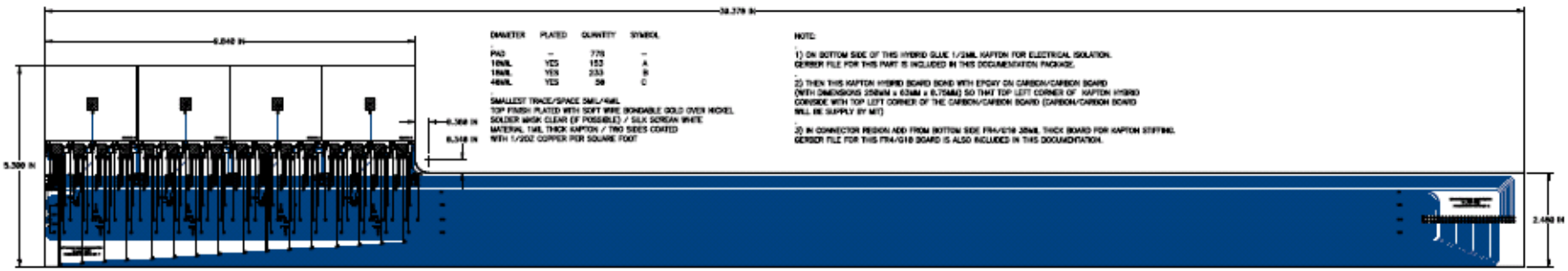
Test Version of FEE for SRAR/IST

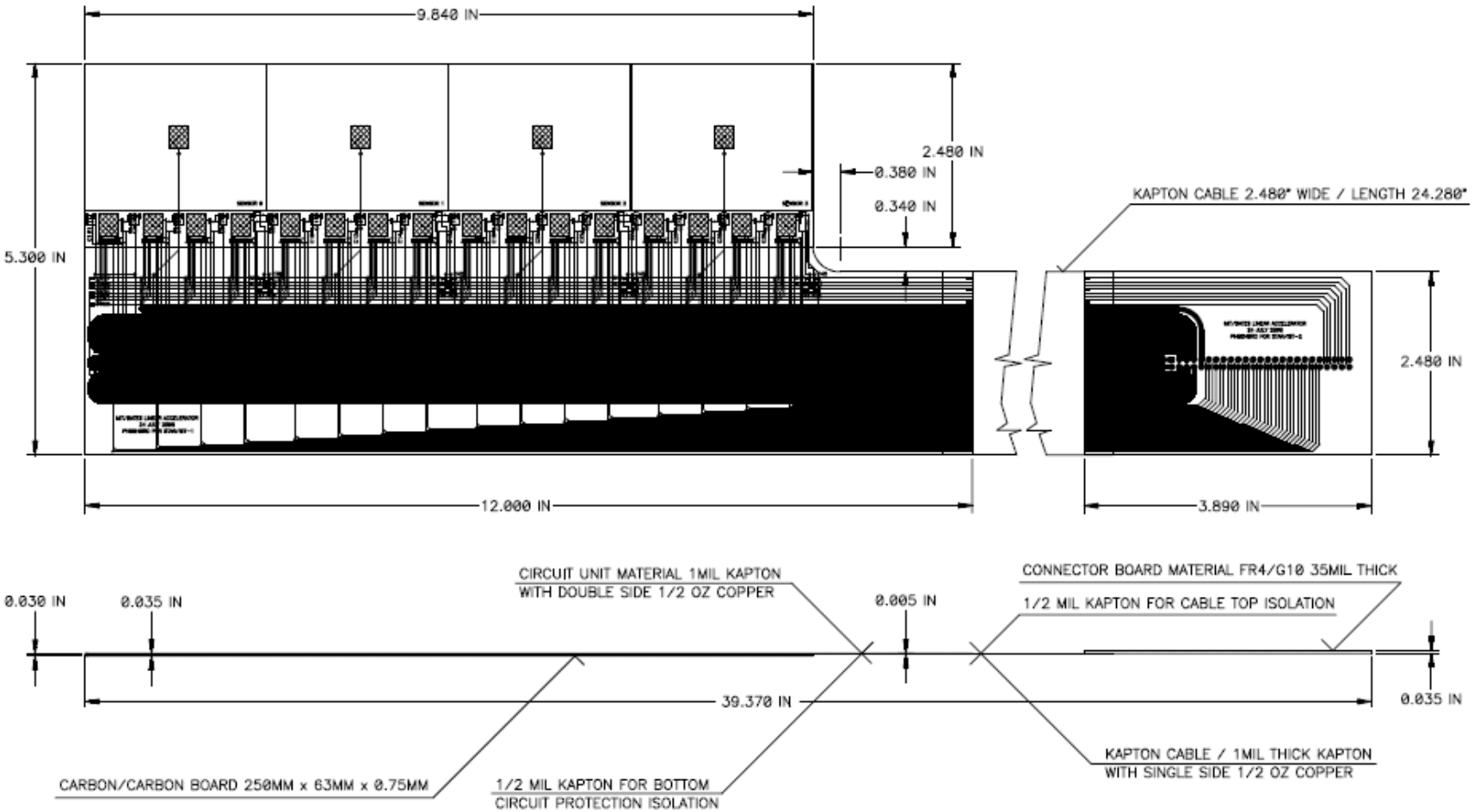
MIT / BATES LINEAR ACCELERATOR

2 October 2008

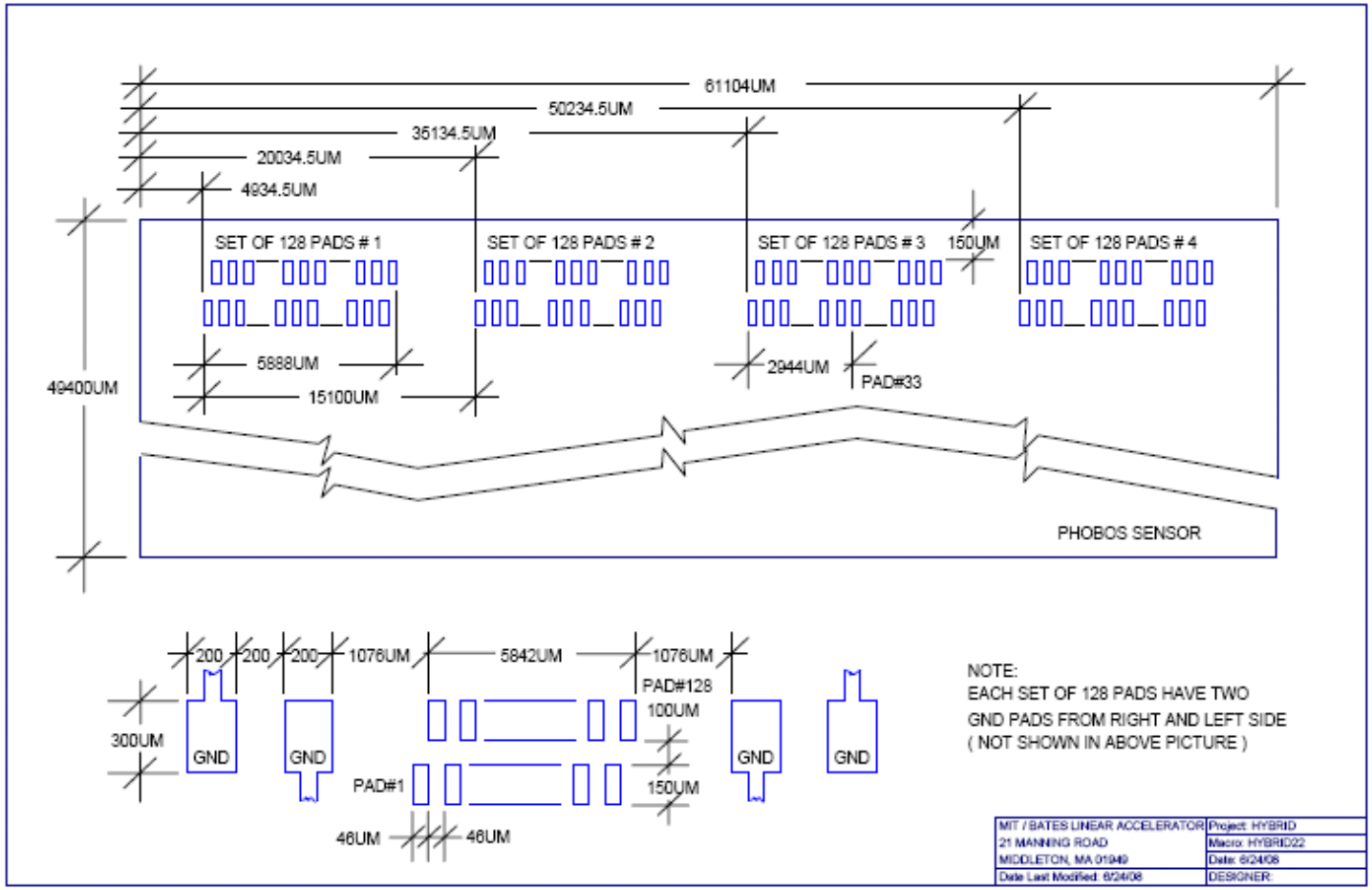
Kapton Hybrid “PHBSHBRD” Version



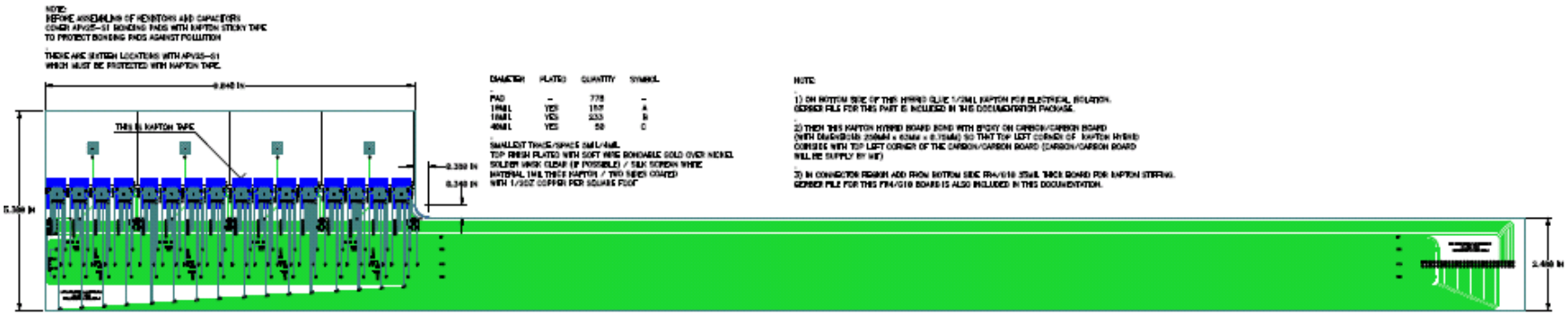
Architecture of 2048 Channel Kapton Hybrid



Phobos Sensor Used in “PHBSHBRD” Test Version

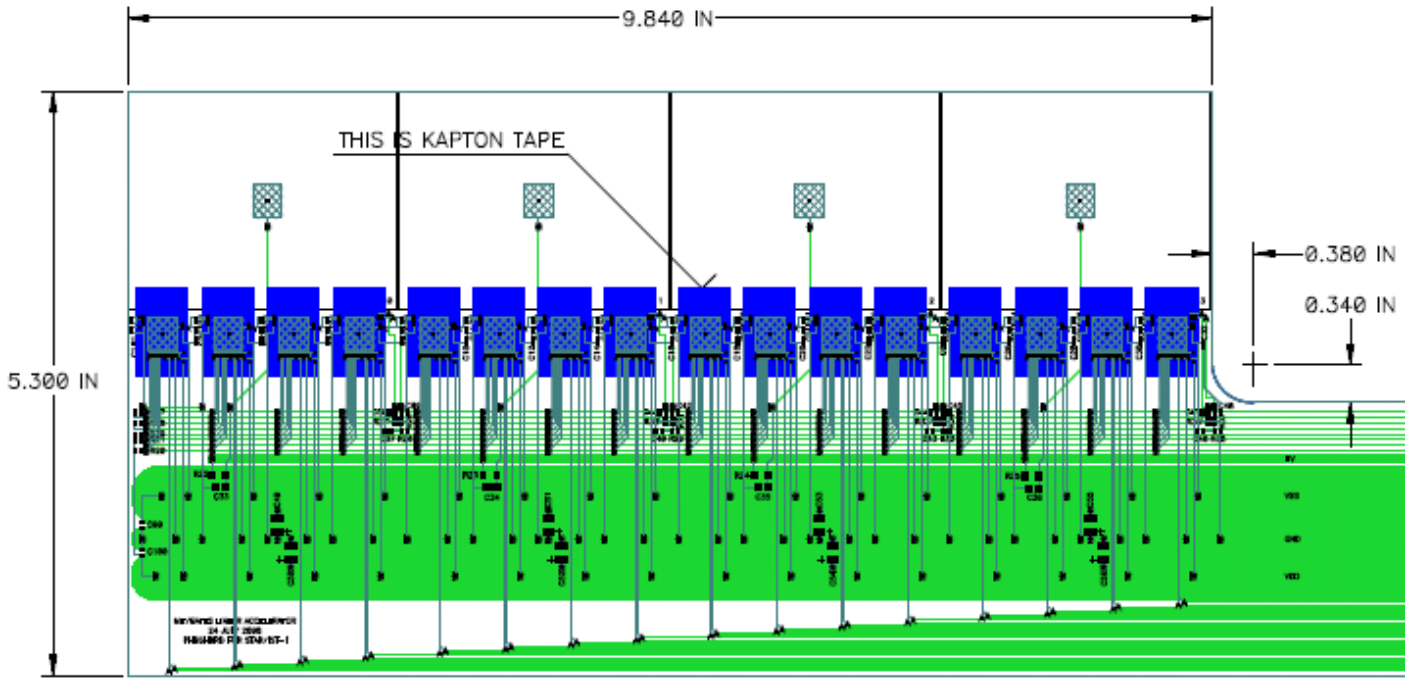


Assembling of “Kapton Hybrid

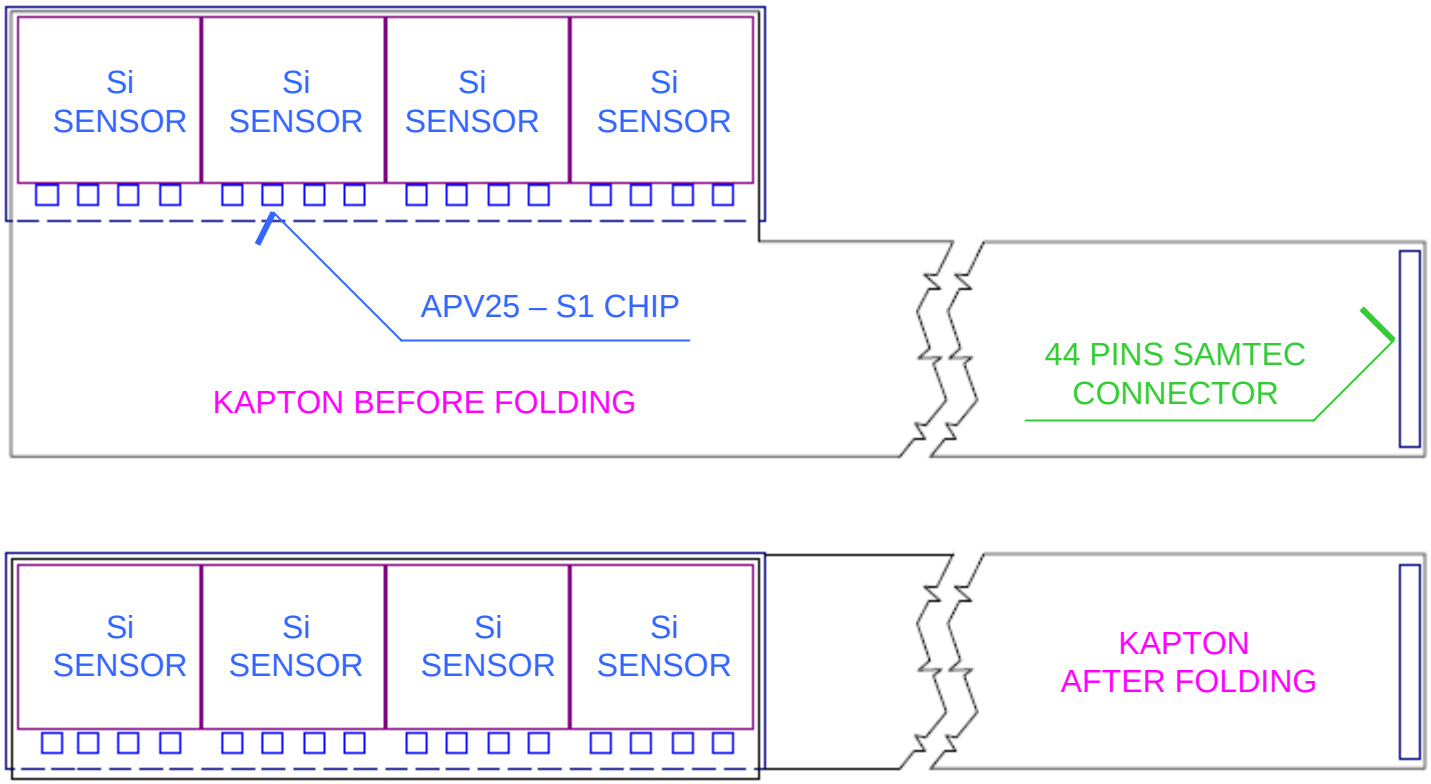


Protection of Bonding Pads During Assembling

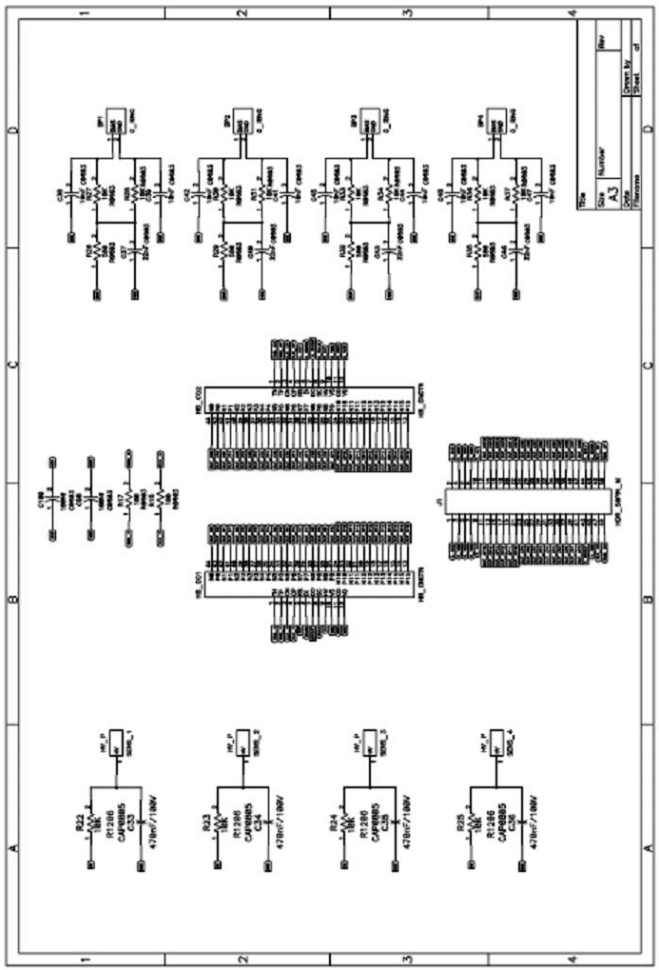
NOTE:
BEFORE ASSEMBLING OF RESISTORS AND CAPACITORS
COVER APV25–S1 BONDING PADS WITH KAPTON STICKY TAPE
TO PROTECT BONDING PADS AGAINST POLLUTION
.
THERE ARE SIXTEEN LOCATIONS WITH APV25–S1
WHICH MUST BE PROTECTED WITH KAPTON TAPE.

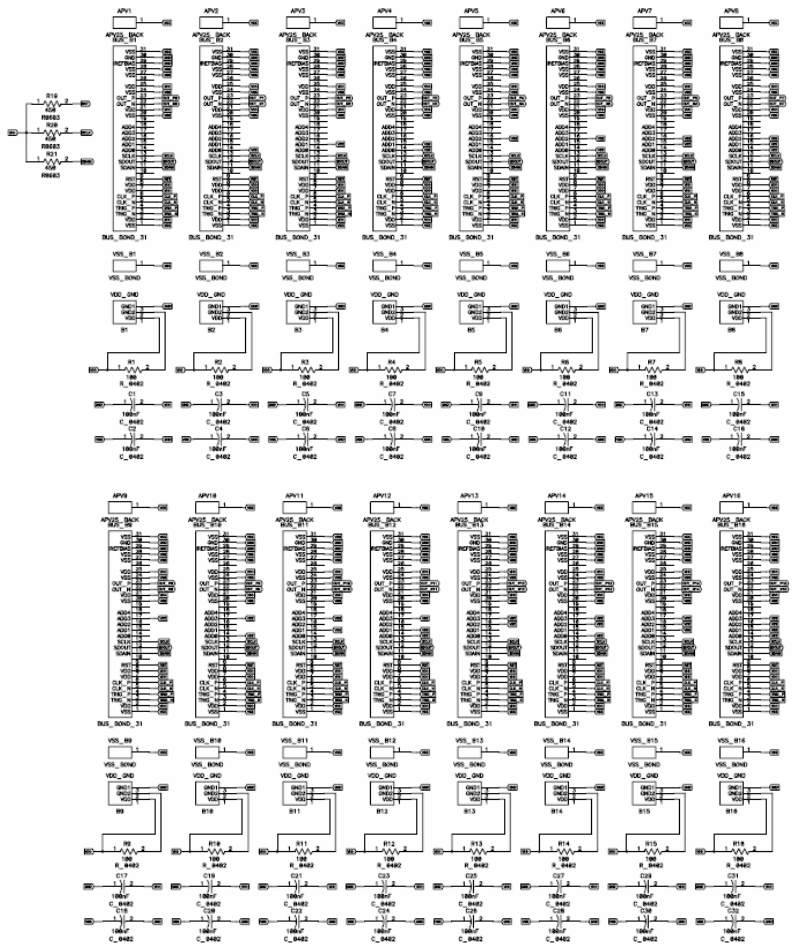


Implementation of Kapton Hybrid in STAR/IST Ladder

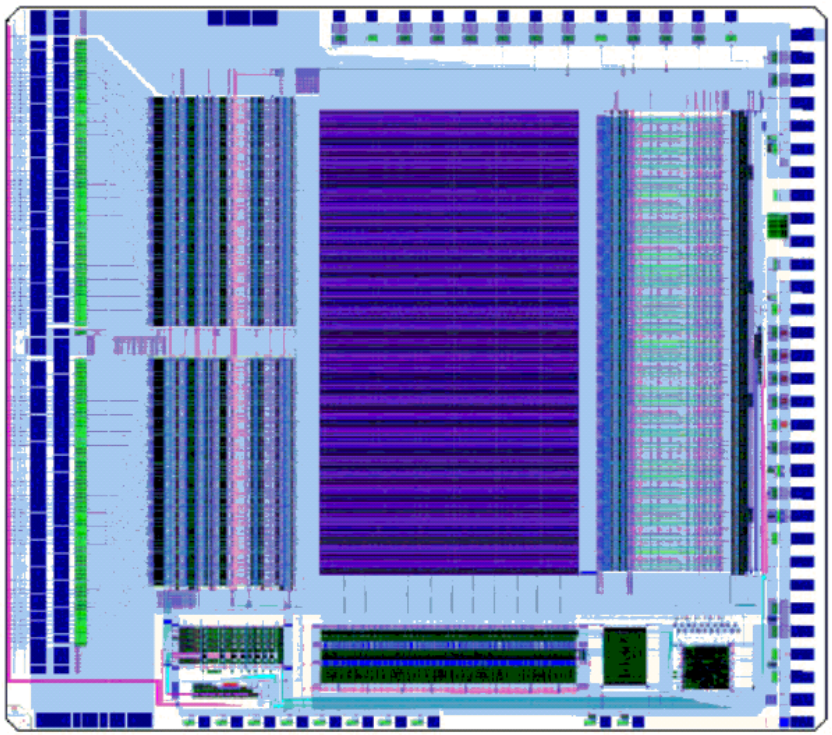


Schematic for Kapton Hybrid





Main Component for FEE is APV25-S1 Chip

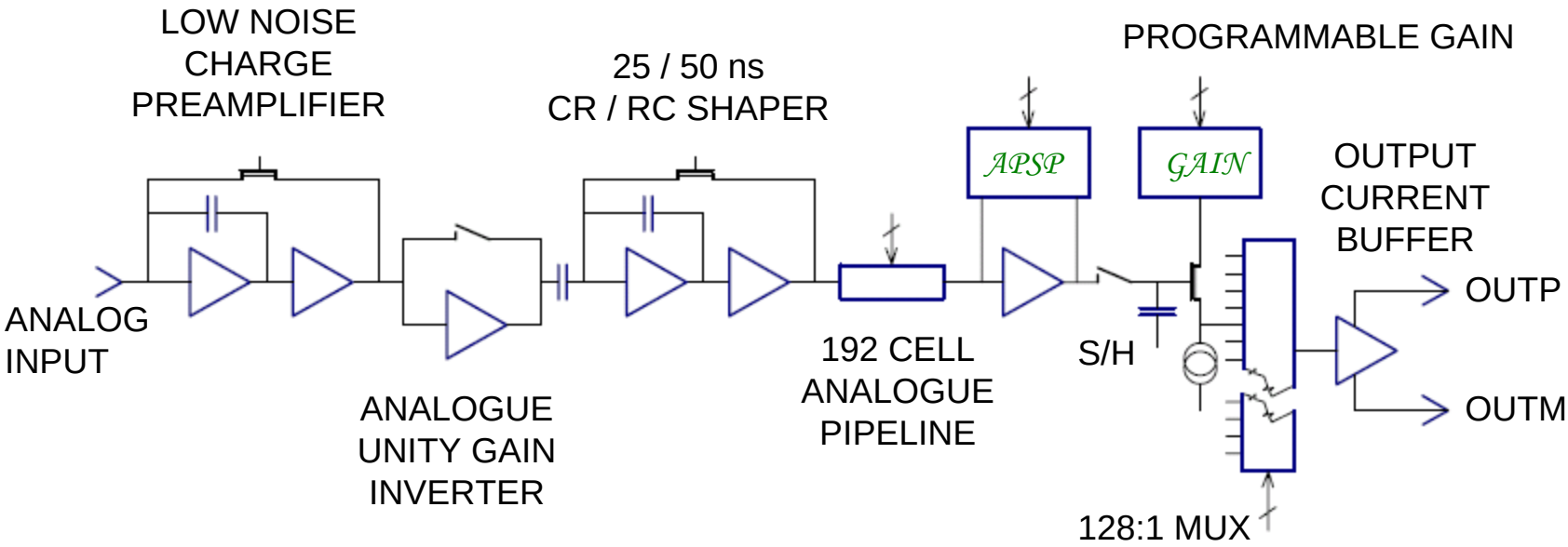


Dimensions 8.1mm x 7.1mm

Fabricated in 0.25um CMOS Process
128 Channels each with
192 Analog Memory Cells

Sampling Frequency 40 MHz
3 Mode of Readout with
25/50ns Shaping Time

Operational Voltage +/- 1.25V
Power Consumption 306mW / Chip

I2C Control / Philips Standard
On Chip Programmable
Bias Generators and Test Pulse

One Channel Architecture of 128 Channels APV25-S1