December 21, 2009

The draft of the Close-out report of the STAR Heavy Flavor Tracker (HFT) Technical, Cost, Schedule and Management (TCSM) Review on November 12-13, 2009 recommends:
"Develop a plan for a ladder system test as soon as possible, using the available MIMOSA-26 chip, which has the architecture fully validated for the needs of STAR. Report draft system test plan to DOE by December 31, 2009."

We have modified our procedures according to this recommendation and herewith submit the draft of a plan for a ladder system test.

Ladder System Test and Development Outline for the PXL Readout Cable

The development of the Pixel detector readout cable is under way. The readout cable, which carries control signals, data signals and power to and from the ten sensors that make up a PXL ladder, is located between the thinned sensor and a carbon fiber stiffener plate. This readout cable is projected to be the single largest contributor to the radiation length of a ladder and thus we will make significant efforts to keep the X_0 as low as possible. An initial design study based on limiting the number of layers in the low mass region of the cable and fitting the power and trace requirements to two sides of a flex PCB indicated that an aluminum conductor based cable could give a radiation length of less than 0.1 %. Using this design concept (http://rnc.lbl.gov/hft/hardware/docs/Phase1/cable_power_gnd_trace_optimization.doc) as the baseline goal, we detail the development steps used to validate cable designs and sensor performance to reach this low X_0 design. A presentation was given detailing this process at an IPHC collaboration meeting in June, 2009: (http://rnc.lbl.gov/hft/hardware/docs/iphc_2009_06/Flex_Cable_Development_LG.ppt) The development of the cable to be used in the prototype Phase-1 based detector will be a four step process with four associated test beds. This prototype cable will serve as the basis for the final sensor cable design. These steps, along with the associated development and testing stages that lead to a prototype Phase-1 and Mimosa-26 based cables, as well as the additional steps leading to the final sensor pixel cable, are listed below. The combination of these ladder cable development prototypes, which will be functionally identical to final detector ladders, and the prototype readout hardware, firmware and software required to read out and analyze the data from these cable test beds, will form a ladder scale system test for the PXL detector.

System Test and Cable Development Sensors

We will use both the Phase-1 and Mimosa-26 sensors in the system test and cable development process. A comparison table of the relevant physical and operating parameters of each sensor is shown below.

Parameter	*Phase-1*	*Mimosa-26*
Clock Frequency	160 MHz	160 MHz
Readout Frequency	160 MHz	160 MHz
LVDS outputs / sensor	4	2
Pixel array size	640 x 640	1152 x 576
Pixel size	30um x 30 um	18.4um x 18.4um
Physical size	~2cm x ~2cm	~ 2cm x ~1cm
Zero suppression	No	Yes – 200 hits/memory array

It is desirable to begin initial infrastructure and system testing with Phase-1 sensors since sensor characterization is much easier when testing sensors without zero suppression incorporated, due to the limited hit memory space of Mimosa-26. The detailed characteristics and basic operation of each sensor may be found in the user manuals. The user manual for the Phase-1 sensor may be found here http://rnc.lbl.gov/hft/hardware/docs/Phase1/PH1-UserMan-20080916.pdf and Mimosa-26 sensor may be found here http://rnc.lbl.gov/hft/hardware/docs/Phase1/M26_UserManual.pdf.
At our current state of development we have all of the required firmware and software to allow for automated testing of ladders of Phase-1 sensors and will begin initial system testing with these sensors. As Mimosa-26 becomes available in quantity, we will modify the testing board layouts and verify our Phase-1 results with the Mimosa-26 sensors and finally with the final PXL sensors.

Infrastructure Test Stage

The goal of this test bed is to evaluate the general design of running 10 sensors on a ladder and find and test the working envelope of bypass capacitance and power supply and ground connection. In this test we will test extensively:

- LVDS clock multi-drop.
- JTAG daisy chain.
- Sensor and system bypass capacitor requirements.
- Power and ground routing and stiffness.
- Noise and cross-talk.
- General operation.

In order to accomplish this testing program, we will produce a large and highly configurable FR-4 based PCB. This testing board will allow for the operation of ten sensors in the running configuration, but with significant additional capabilities that will not be available on a ladder sized PCB. The envisioned board configuration capabilities include:

- Analog readout available from all sensors (RDO limit is one sensor or 8 channels at a time)
- Jumper selectable power source to each individual sensor.
- In series replaceable resistor for each sensor power supply (analog and digital)
- Removable board level capacitor bypassing.
- Removable individual sensor capacitor bypassing.
- Readout over 2m fine wire as per final ladders.
- Readout through the full HFT data path including Mass Termination Boards (MTB).
- All buffering and drivers use the same chips as the final ladder.

We will initially equip this test board with probe-tested and characterized Phase-1 sensors. We will vary the operating parameters while monitoring each sensor on the ladder for deviation from its individually tested characteristics. It is expected that this testing will be comprehensive and result in an understood set of operational parameters and parameter envelope for sets of ten sensors operated in a ladder configuration. This will be necessary for the next phase of cable development.

Production Prototype in FR-4 with Cu Conductor

Taking the knowledge gained in the Infrastructure Test Phase, we now attempt to fit the readout cable traces into the required size of the ladder readout cable. The object of this test is to produce a real size FR-4 PCB with Cu conductor that contains the layout and signal paths that we will use for the final detector. In addition to the full functionality testing, this will allow for the full data path testing as well as optimizing the wire bonding and assembly development and testing. In addition, all testing stages from this stage on will be tested with the carbon fiber stiffener plate in place. This production prototype is expected to have the following attributes:

- Correct size and the same layout geometry as the final cable.
- The testing of this cable is via digital output only. All other testing functionality removed.
- Prototype of final termination, JTAG daisy chain and capacitive bypassing scheme.
- All buffering and drivers use the same chips as the final ladder.
- Power provided from MTBs.
- Readout over 2m fine wire as per final ladders.
- We will attempt to have the thickness of the Cu layer mimic the final cable to give the correct power and ground impedances.

The testing of this cable is via digital output only. General function will be tested as well as discriminator transfer function widths and noise as compared to the probe test results from the sensor prior to their loading onto the cable. It is anticipated that this design may take multiple iterations to troubleshoot and optimize.

Production Prototype in Kapton with Cu conductor

This cable is a pre-production cable in Kapton with Cu traces and is the direct translation of the previous stage cable into a Kapton flex cable design. This will involve some reshaping of via entries and other automated kapton flex design translations from standard FR-4 PCB design. The attributes and testing plan for this stage are as above in the FR-4 version. It is expected that we will be using this cable extensively in the production prototyping process.

Production (Final PXL) Cable in Kapton with Cu Conductor

After the successful development of the Phase-1 based prototype cable, we expect the transition to the PXL final sensor cable design to be relatively simple. The number of digital differential output pairs will have decreased by half. The power requirements will have only modestly increased. We will examine the operation envelope in the individual testing phase and compare it to the Phase-1 sensor. The final PXL sensor shares all of the attributes of the Phase-1 sensor but has additional on-chip zero-suppression. The readout speed remains the same at 160 MHz. The cable development for the final PXL sensor will follow the same path as the last two phases of the Phase-1 development.

Production (Final PXL) Cable in Kapton with Al Conductor

As before, after the successful implementation in Kapton with Cu conductor, we will move to Al conductor based fabrication. It is desired that we make an early start on pre-production designs and iterate with the manufacturer so that any production difficulties encountered in the initial manufacturing can be understood and overcome.

System Test Firmware and Software Development

The development paths of the software and firmware parallel the development path of the hardware for the sensor ladder cable development and system testing. In the initial infrastructure testing, we will begin with our existing functional individual sensor readout firmware and software. We will then extend the readout firmware and software (from one to multiple parallel streams) to full ladders of 10 sensors using the infrastructure test bed to validate the firmware/software development effort. A successful completion of the initial infrastructure test requires having working ladder readout firmware and software. Firmware and software changes to allow for reading different sensor output formats due to the incorporation of zero-suppression on post Phase-1 generations of sensors will be built in natively to the software and firmware design and implemented as a pre-processing firmware module that implements the IPHC zero-suppression scheme. This pre-processing module will be used when reading out Phase-1 based ladders. This allows us to keep all downstream firmware and software the same for all currently envisioned generations of sensors.

Schedule, Effort and Deliverables

This development effort is scheduled for the current FY10 year and is underway. It is expected to be complete by Q1FY11. The effort can be found in the HFT Pixel cost estimation sheets presented in the HFT CD-1 review. The relevant WBS items are presented below:

1.2.2.3.1 Infrastructure Test Cable
1.2.2.3.2 Prototype Ladder Cable (FR-4)
1.2.2.3.3 Ladder Cable (Kapton with Cu conductor)
1.2.2.5.1 firmware and software (PH-1 readout)

The total effort summed over the above WBS items is shown below .The items and their associated costs are included in the project base costs presented at the pre-CD1 review.

Material	Tech (hr)	Postdoc (hr)	Engineer (hr)	Eng. cont (hr)
70 k$	512	1324	288	1830

The final deliverable from this prototyping effort is a working system test-bed consisting of

- Written report detailing testing described above and indicating the expected operating envelope of ladders of sensors.
- Working infrastructure test board with 10 working sensors.*
- Working production prototype test board in FR4 with 10 working sensors.*
- Working production prototype test board in Kapton with 10 working sensors.*
- Prototype firmware and software for reading out and analyzing data from 10 sensor ladders.
- RDO hardware including prototype Mass Termination Boards (MTB) and RDO motherboards with all cabling required for readout.

* having 10 working sensors/ladder is contingent on successful development of probe testing to allow us to select only working sensors to mount to ladders.