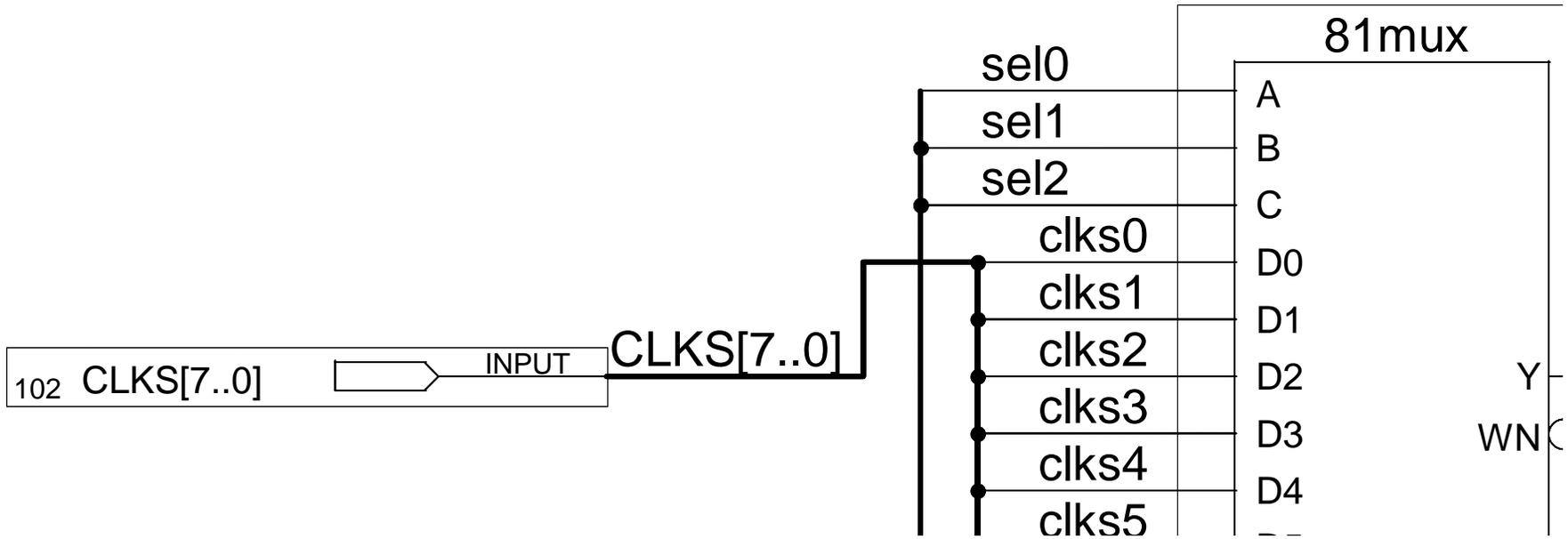
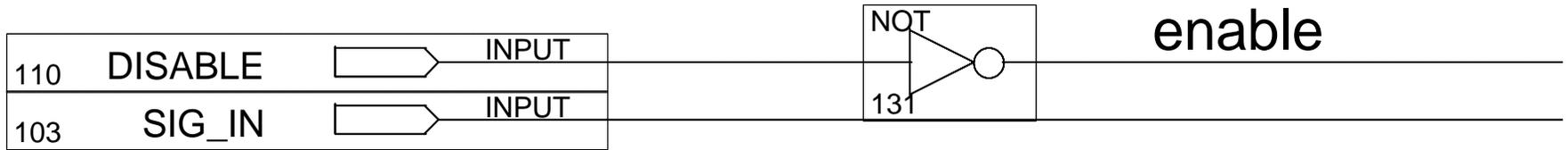
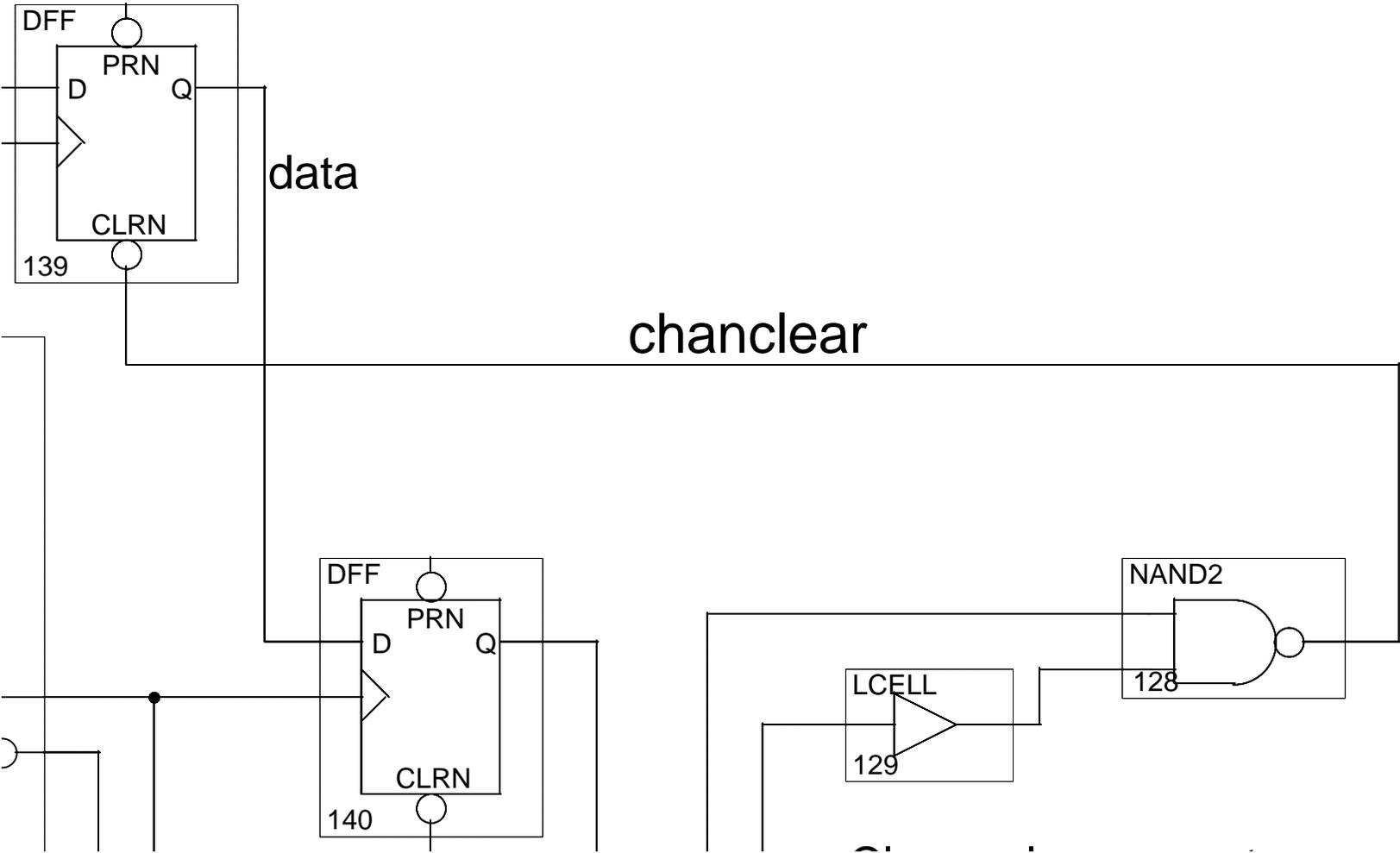
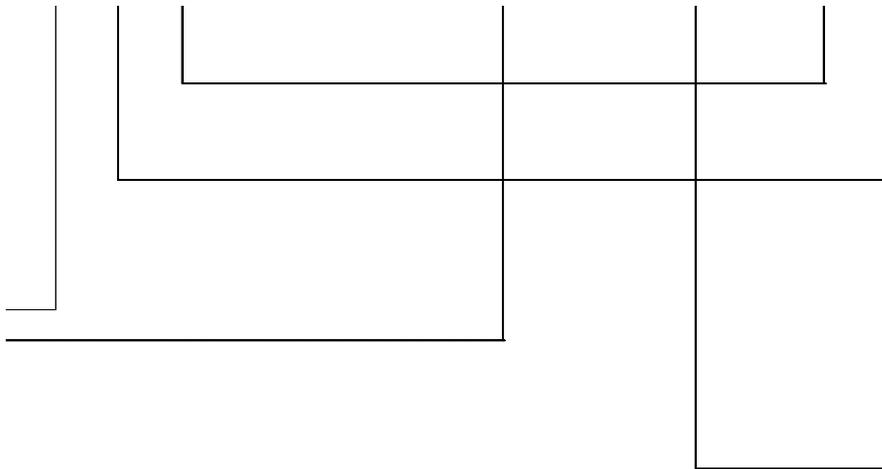


Select the desired skew on the input clocks to delay the input signal. The SIG\_IN signal is latched asynchronously. This data is clocked when the delayed beam clock arrives. This edge also clears the input signal flip-flop. If the HALT line is asserted, the input CLKS are blocked and the output does not change. The "data" line, however, is still enabled and can change during this HALT time. The first set of data sent out after the HALT state is removed will not be good as many of the lines may have gone high.





# Clear pulse generator



out

3

TITLE		8DMUX - Single channel input signal delay			
COMPANY		ORNL			
DESIGNER		Ganesh S. Rao			
SIZE	B	NUMBER	1.00	REV	A
DATE	2:13p 3-20-1998			SHEET	1 OF 1
104					