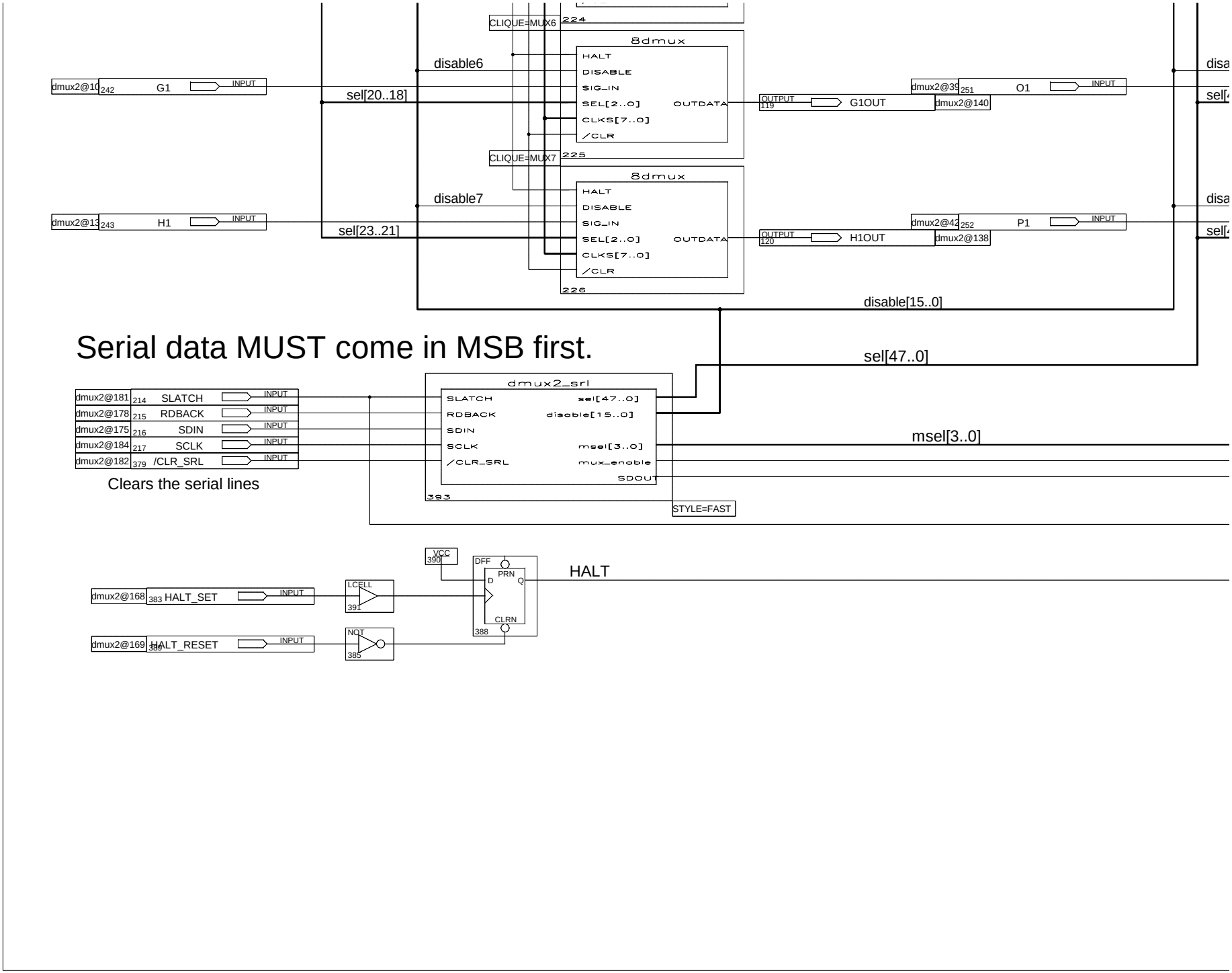
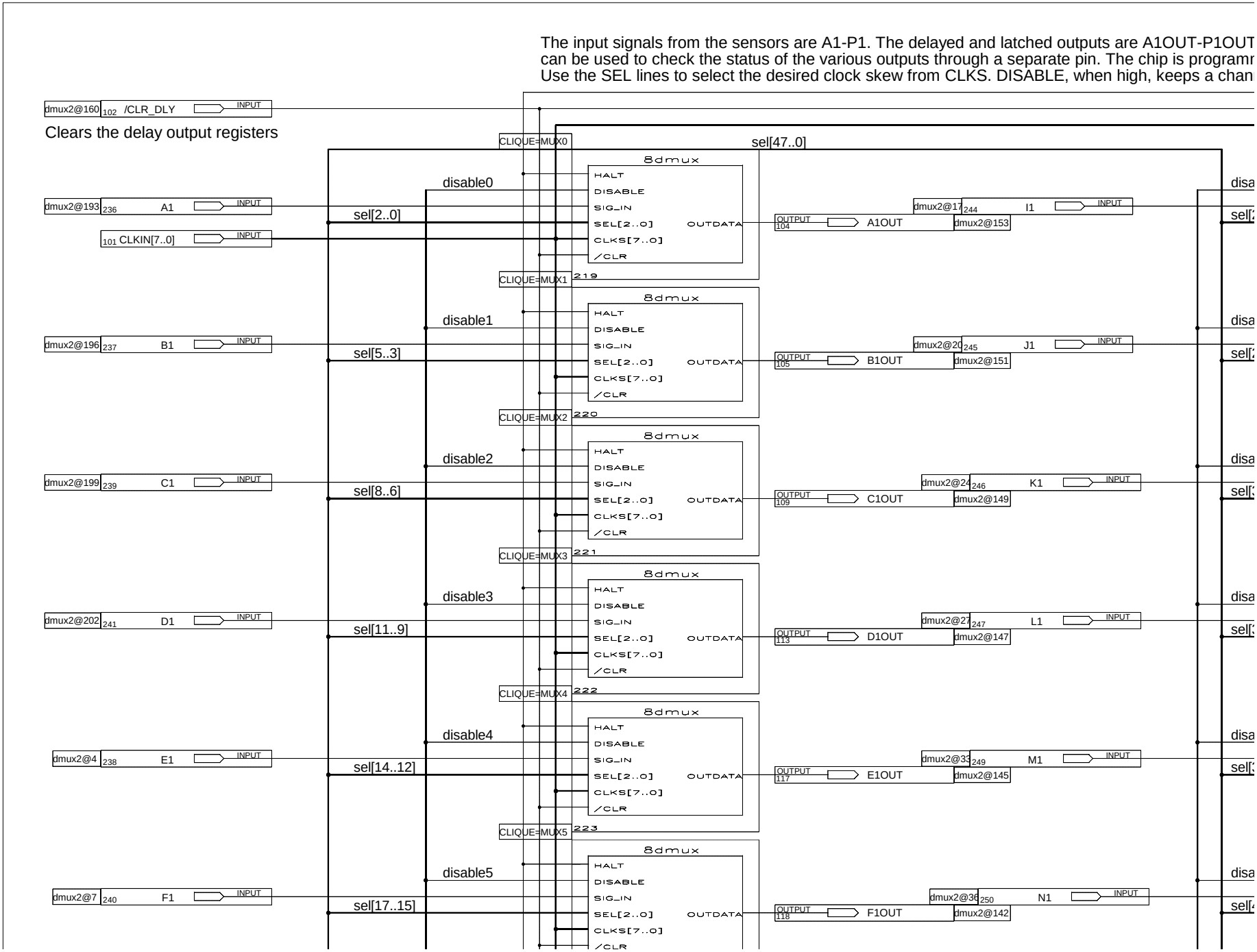
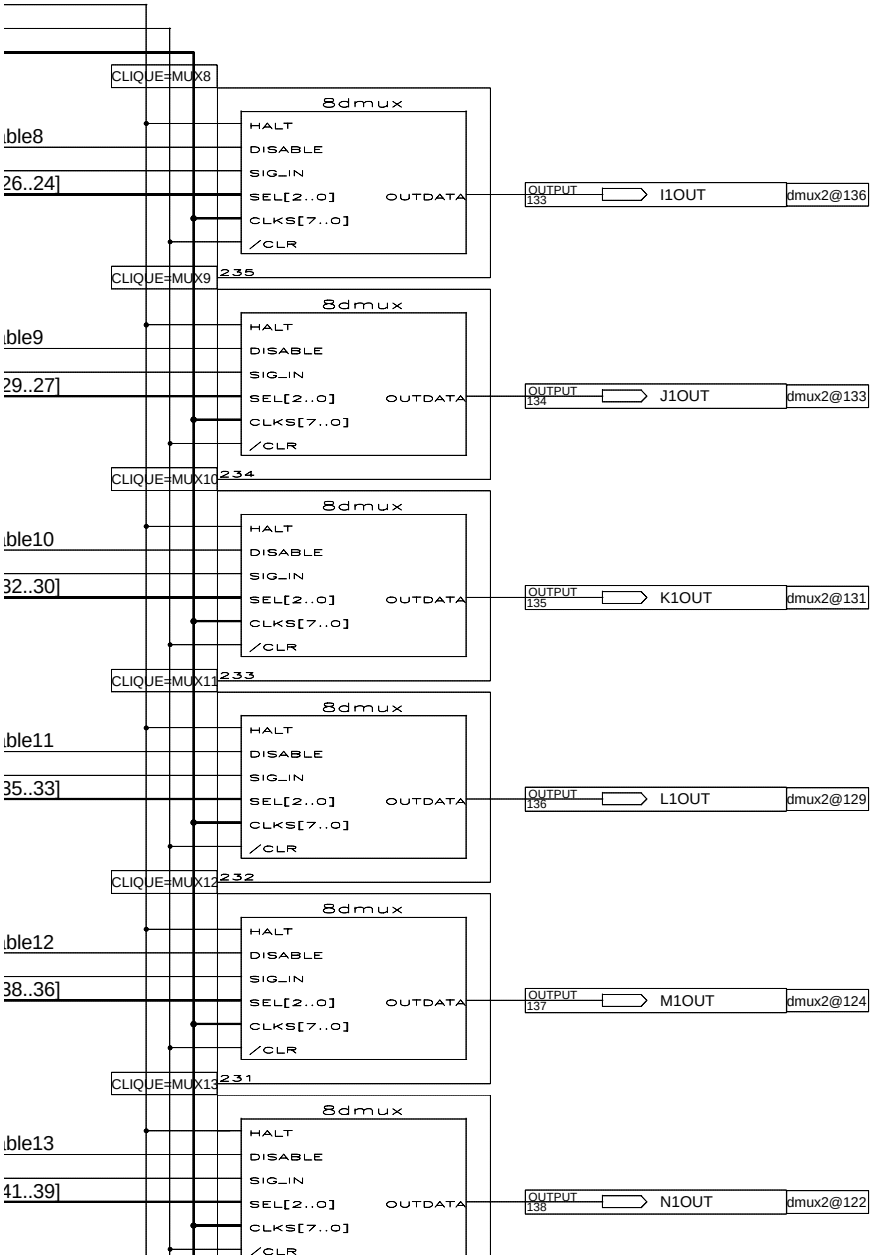
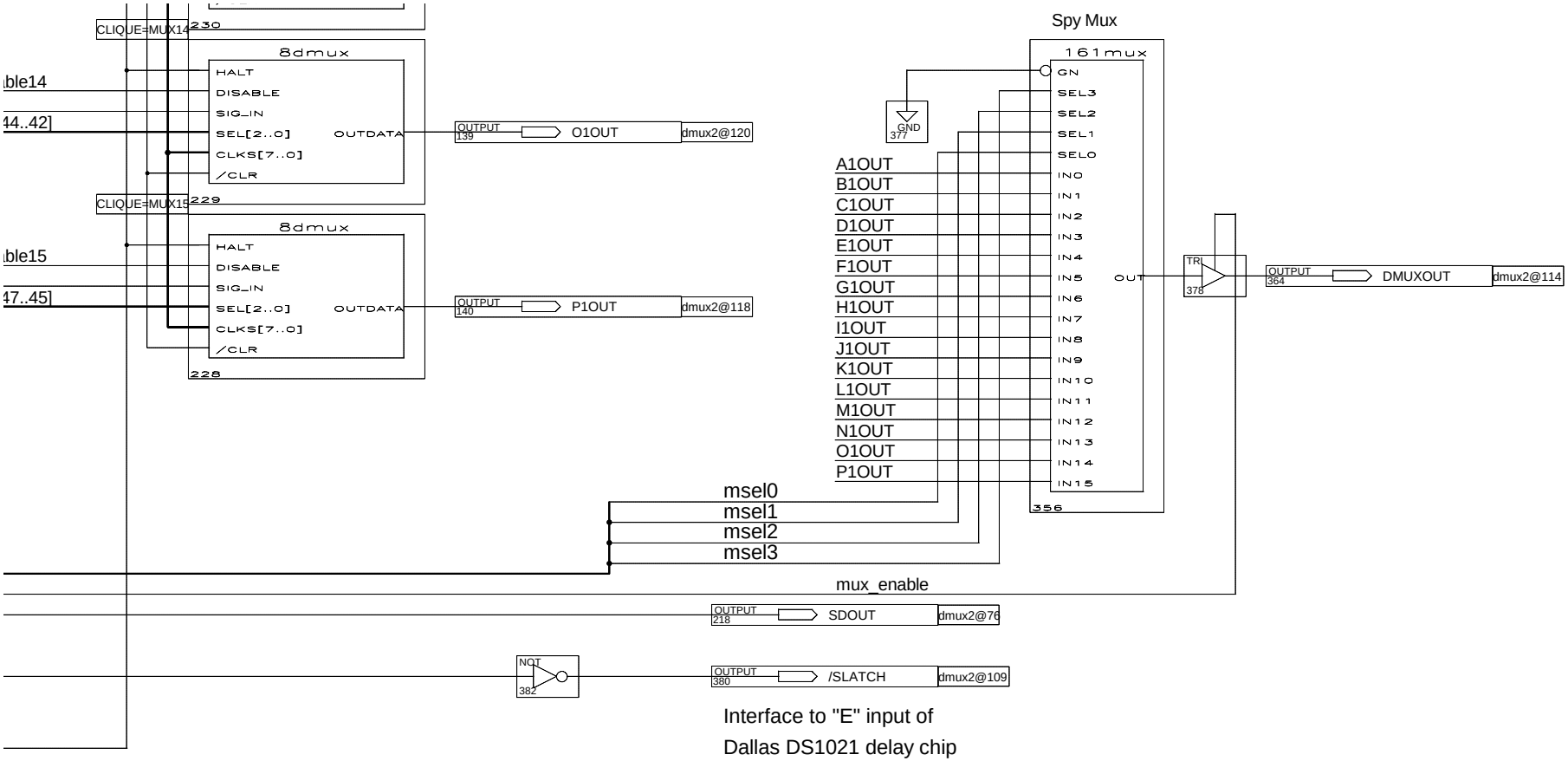

CLIQUE=MUX6
224
8dmux
HALT
DISABLE
SIG_IN
SEL[2..0]
OUTDATA
CLKS[7..0]
/CLR
disable6
dmux2@10
242
G1
INPUT
sel[20..18]
OUTPUT
119
G1OUT
dmux2@39
251
O1
INPUT
dmux2@140
CLIQUE=MUX7
225
disable7
dmux2@13
243
H1
sel[23..21]
OUTPUT
120
H1OUT
dmux2@42
252
P1
dmux2@138
226
disable[15..0]
Serial data MUST come in MSB first.
sel[47..0]
dmux2@181
214
SLATCH
dmux2@178
215
RDBACK
dmux2@175
216
SDIN
dmux2@184
217
SCLK
dmux2@182
379
/CLR_SRL
Clears the serial lines
dmux2_srl
SLATCH
RDBACK
SDIN
SCLK
/CLR_SRL
sel[47..0]
disable[15..0]
msel[3..0]
mux_enable
SDOUT
393
STYLE=FAST
VCC
390
DFF
PRN
D
Q
CLRN
388
HALT
dmux2@168
383
HALT_SET
LCELL
391
dmux2@169
HALT_RESET
NOT
385


The input signals from the sensors are A1-P1. The delayed and latched outputs are A1OUT-P1OUT
can be used to check the status of the various outputs through a separate pin. The chip is programm
Use the SEL lines to select the desired clock skew from CLKS. DISABLE, when high, keeps a chan
dmux2@160 102 /CLR_DLY INPUT
Clears the delay output registers
CLIQUE=MUX0
sel[47..0]
8dmux
HALT
DISABLE
SIG_IN
SEL[2..0]
CLKS[7..0]
/CLR
OUTDATA
disable0
dmux2@193 236 A1 INPUT
sel[2..0]
101 CLKIN[7..0] INPUT
CLIQUE=MUX1 219
disable1
dmux2@196 237 B1 INPUT
sel[5..3]
CLIQUE=MUX2 220
disable2
dmux2@199 239 C1 INPUT
sel[8..6]
CLIQUE=MUX3 221
disable3
dmux2@202 241 D1 INPUT
sel[11..9]
CLIQUE=MUX4 222
disable4
dmux2@4 238 E1 INPUT
sel[14..12]
CLIQUE=MUX5 223
disable5
dmux2@7 240 F1 INPUT
sel[17..15]
OUTPUT 104 A1OUT dmux2@153
OUTPUT 105 B1OUT dmux2@151
OUTPUT 109 C1OUT dmux2@149
OUTPUT 113 D1OUT dmux2@147
OUTPUT 117 E1OUT dmux2@145
OUTPUT 118 F1OUT dmux2@142
dmux2@17 244 I1 INPUT
dmux2@20 245 J1 INPUT
dmux2@24 246 K1 INPUT
dmux2@27 247 L1 INPUT
dmux2@33 249 M1 INPUT
dmux2@36 250 N1 INPUT

. The digital Spy Mux
ned serially.
nel from firing.





TITLE	DMUX - Delay lines for 16 input channels		
COMPANY	ORNL		
DESIGNER	Ganesh S. Rao		
SIZE E	NUMBER 1.00	REV A	
DATE 354 1:58p 3-20-1998		SHEET 1	OF 1