

15 BCLR 86

Data is clocked into FIFO on rising edges of Beam Clock

45 /CLR_FIFO INPUT

This clears the FIFOs and the output is reset (tri-stated).

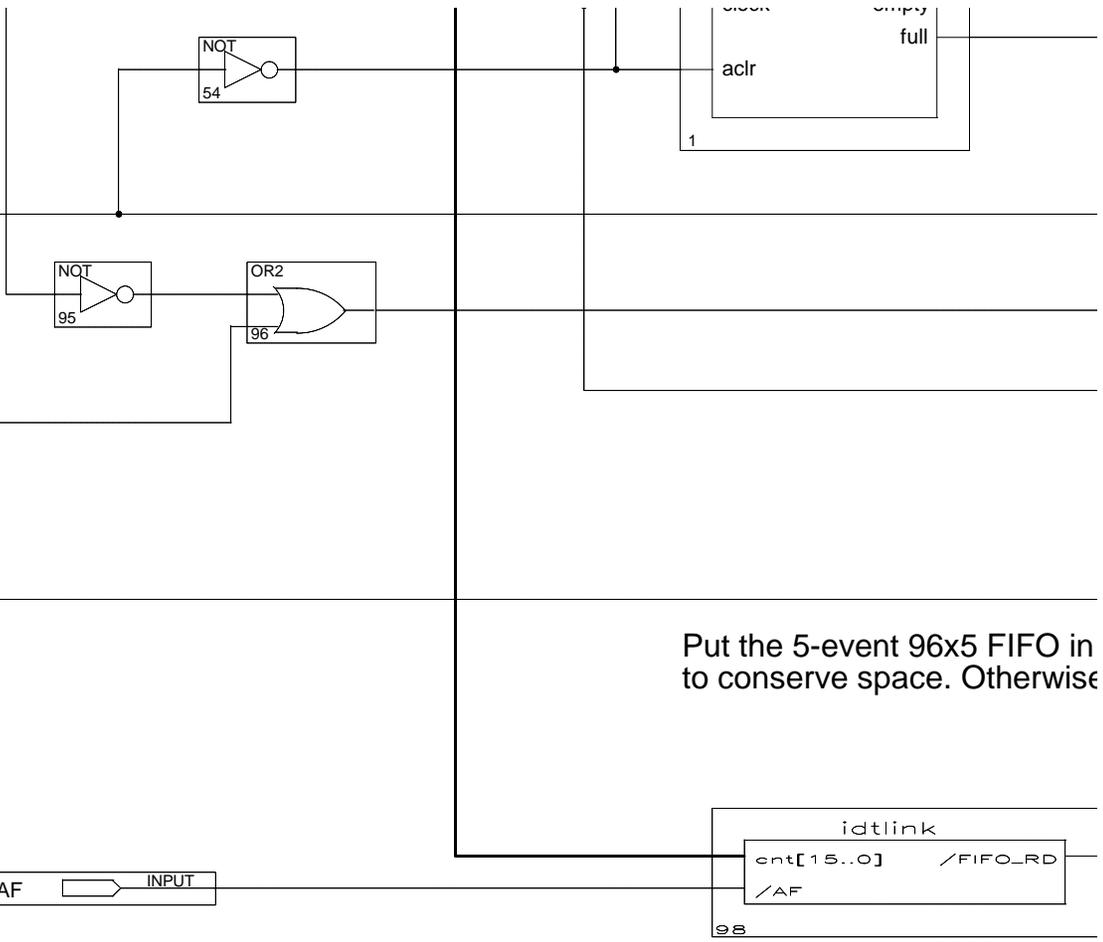
71 /RDEN INPUT

/RDEN (from ADDR & /ALE) must be LOW for entire read cycle to enable outputs.

4 /RD INPUT

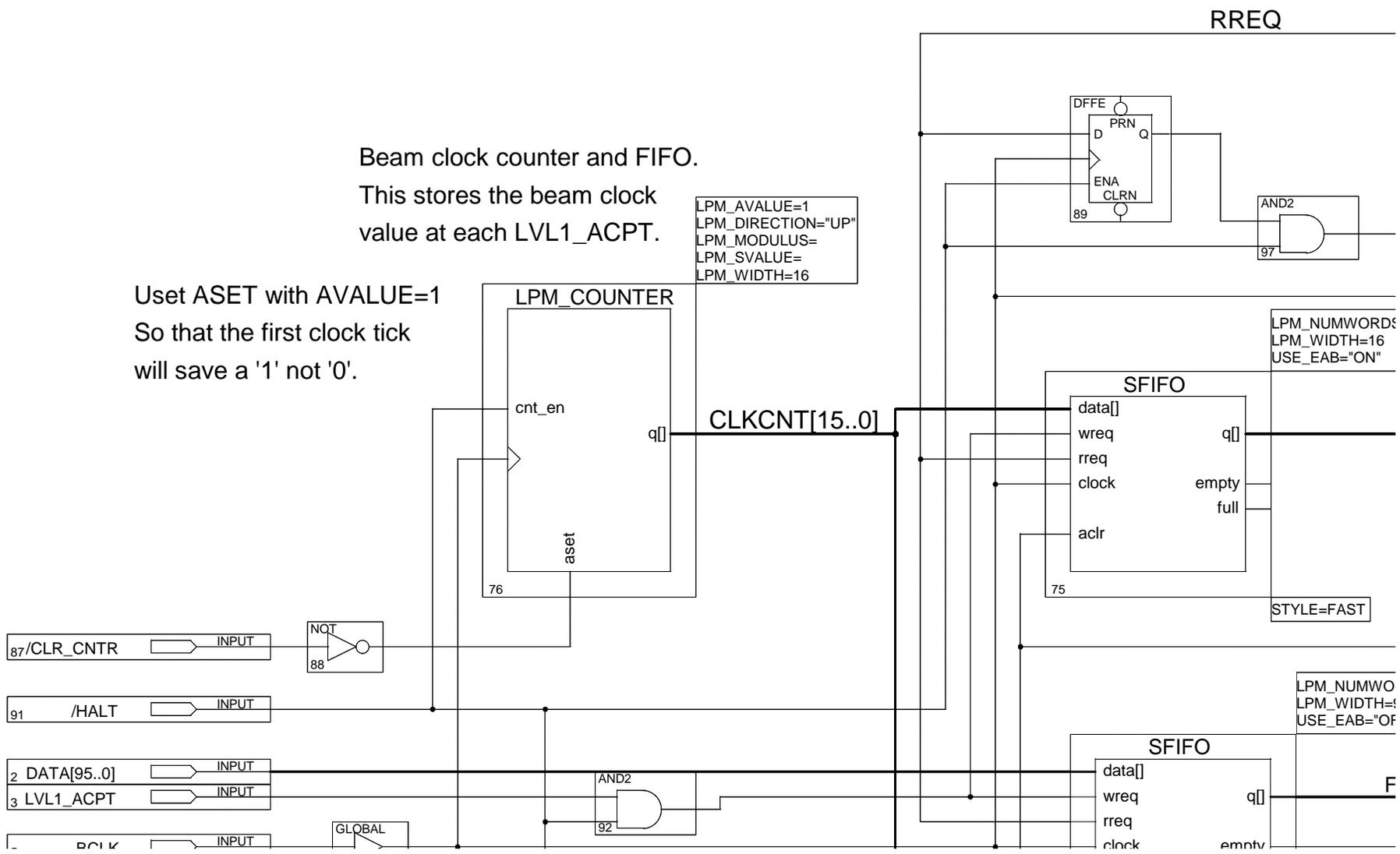
Each low-going /RD pulse enables the next 16-bit data word onto the output bus.

eventfifo@150 99 /AF INPUT



Put the 5-event 96x5 FIFO in to conserve space. Otherwise

Interface to the IDT FIFO. 1 external data FIFO to a cor



Beam clock counter and FIFO.
This stores the beam clock
value at each LVL1_ACPT.

Uset ASET with AVALUE=1
So that the first clock tick
will save a '1' not '0'.

LPM_AVALUE=1
LPM_DIRECTION="UP"
LPM_MODULUS=
LPM_SVALUE=
LPM_WIDTH=16

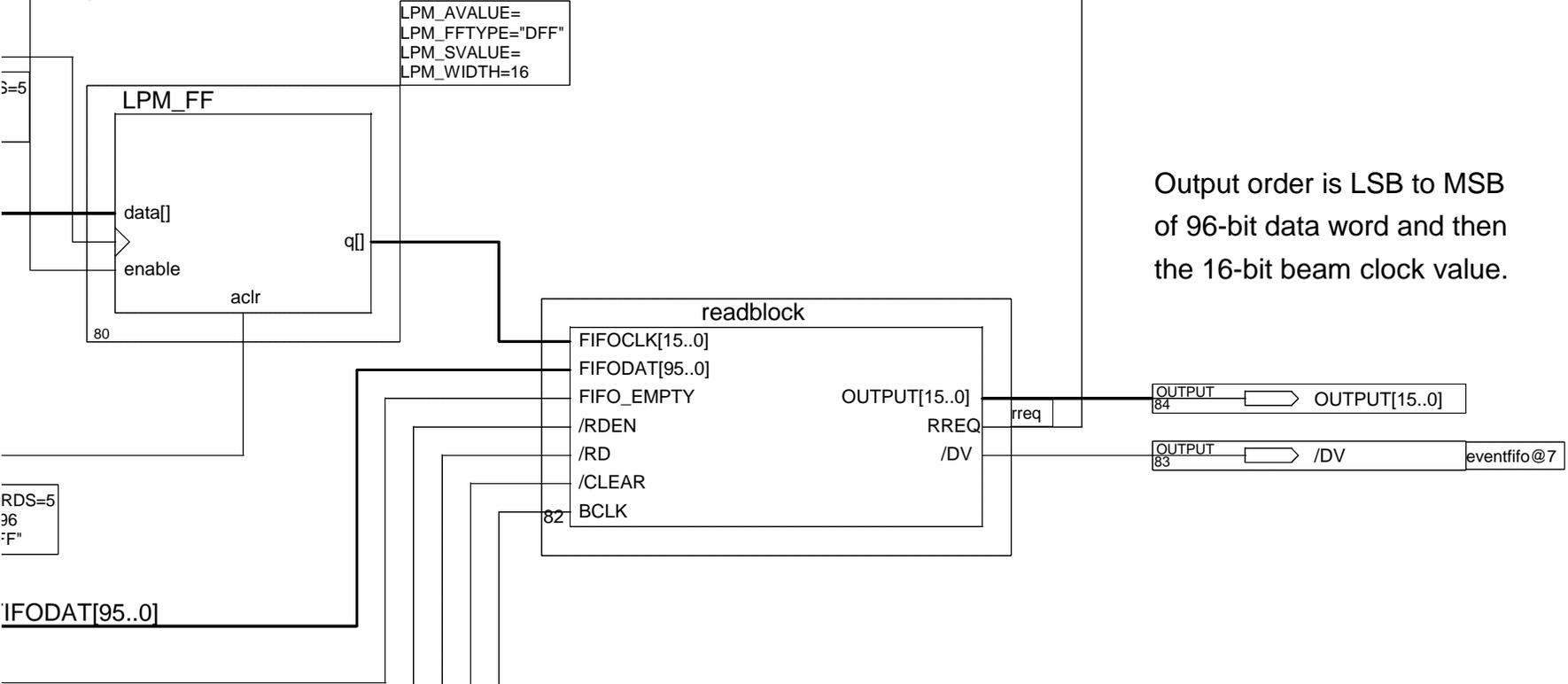
LPM_NUMWORDS=16
LPM_WIDTH=16
USE_EAB="ON"

STYLE=FAST

LPM_NUMWORDS=16
LPM_WIDTH=16
USE_EAB="OF"

F

The D-flops are required at the output because this FIFO is in the EAB. Without them, the next BCLK cycle will clear the outputs. This is not true of the 5-event FIFO as it is in the LABs. Also, optimize this FIFO for speed in the logic options. This removes any setup/hold errors.



Output order is LSB to MSB of 96-bit data word and then the 16-bit beam clock value.



The /DV output is active low and valid only if one of the 6 data words is being output AND the fifo was not empty when the last read was performed. The line goes high (invalid) when the Beam Clock counter is written out.

the LABs and not the EAB, a very huge part will be needed.



This block limits the depth of the instant amount specified within the block.

TITLE				EventFIFO - The 5-event FIFO			
COMPANY				ORNL			
DESIGNER				Ganesh S. Rao			
SIZE	D	NUMBER	1.00	REV	A		
DATE	4:37p 3-17-1998			SHEET	1	OF	1
60							