



Use ASET with AVALUE=1  
So that the first clock tick  
will save a '1' not '0'.

Beam clock counter and FIFO.  
This stores the beam clock  
value at each LVL1\_ACPT.

Data is clocked into FIFO on  
rising edges of Beam Clock

This clears the FIFOs and the output  
is reset (tri-stated).

/RDEN (from ADDR & /ALE) must be  
LOW for entire read cycle to  
enable outputs.

Each low-going /RD pulse enables the  
next 16-bit data word onto the output bus.

Put the 5-event 96x5 FIFO in the LABs and not the EAB  
to conserve space. Otherwise, a very huge part will be needed.

Interface to the IDT FIFO. This block limits the depth of the  
external data FIFO to a constant amount specified within the block.

The D-flops are required at the output because this FIFO is in the EAB.  
Without them, the next BCLK cycle will clear the outputs. This is not true of the  
5-event FIFO as it is in the LABs. Also, optimize this FIFO for speed in the  
logic options. This removes any setup/hold errors.

Output order is LSB to MSB  
of 96-bit data word and then  
the 16-bit beam clock value.

The /DV output is active low and  
valid only if one of the 6 data words  
is being output AND the fifo was not  
empty when the last read was performed.  
The line goes high (invalid) when the  
Beam Clock counter is written out.

TITLE				EventFIFO - The 5-event FIFO			
COMPANY				ORNL			
DESIGNER				Ganesh S. Rao			
SIZE	D	NUMBER	1.00	REV	A		
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