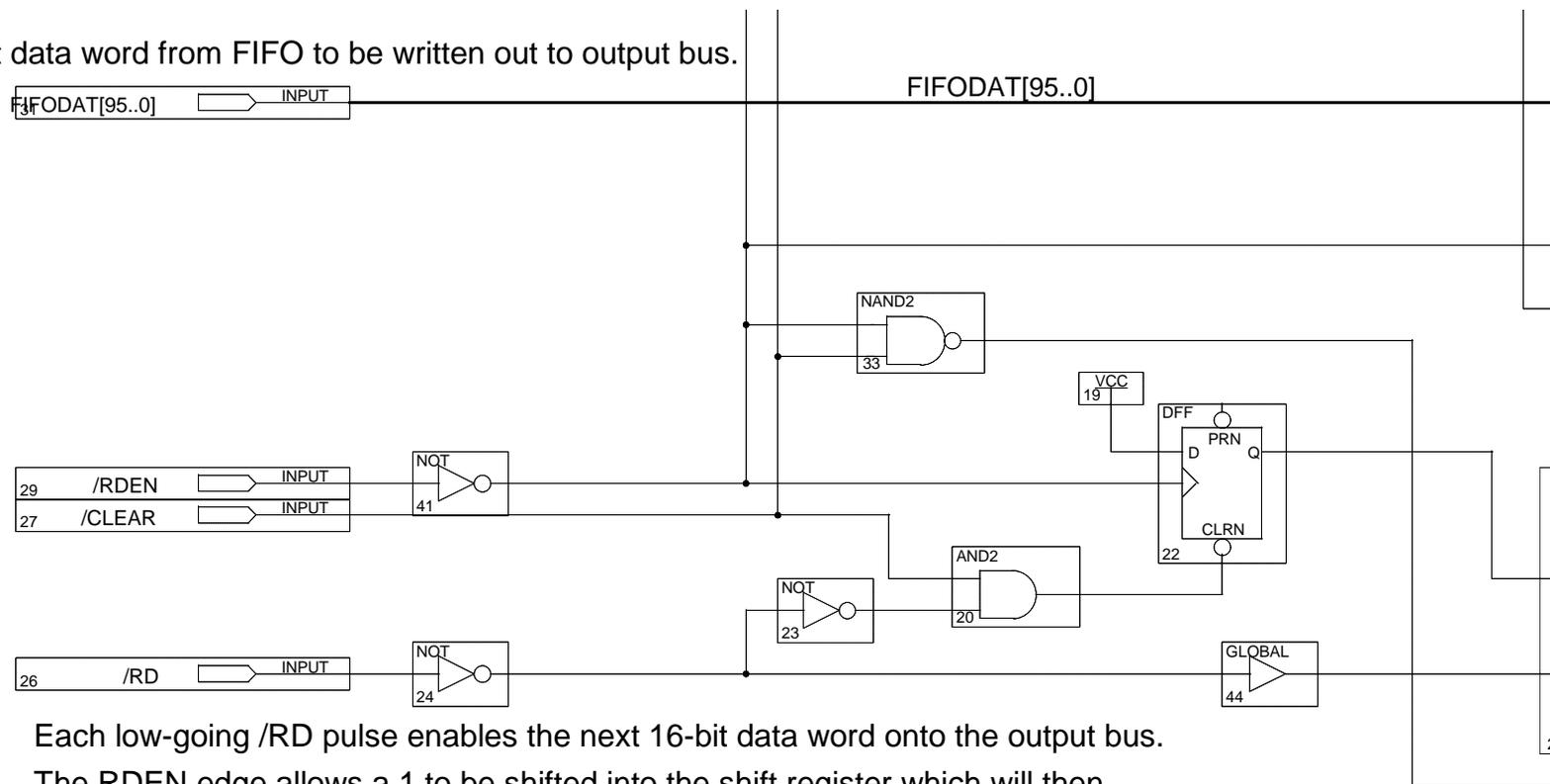


96-bit data word from FIFO to be written out to output bus.



Each low-going `/RD` pulse enables the next 16-bit data word onto the output bus. The `RDEN` edge allows a 1 to be shifted into the shift register which will then enable one 16-bit output word at a time. The first `/RD` pulse clears the "shiftin" input so only one "1" is shifted in per read cycle.

Beam Clock data from FIFO to be written out to output bus.

FIFOCLK[15..0] INPUT

FIFOCLK[15..0]

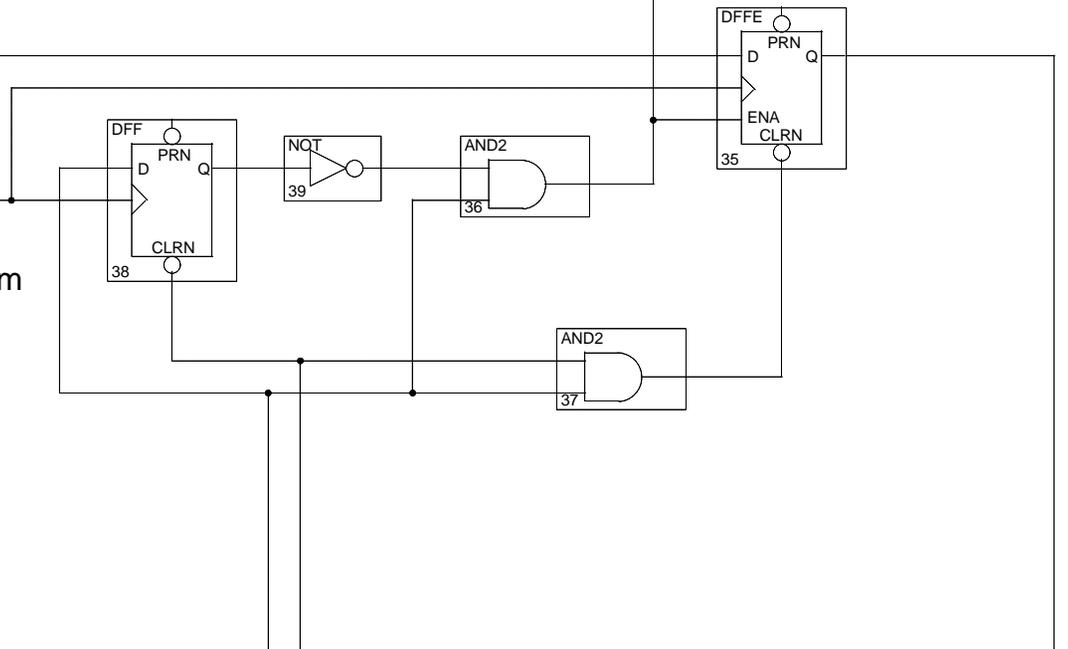
FIFO empty flag

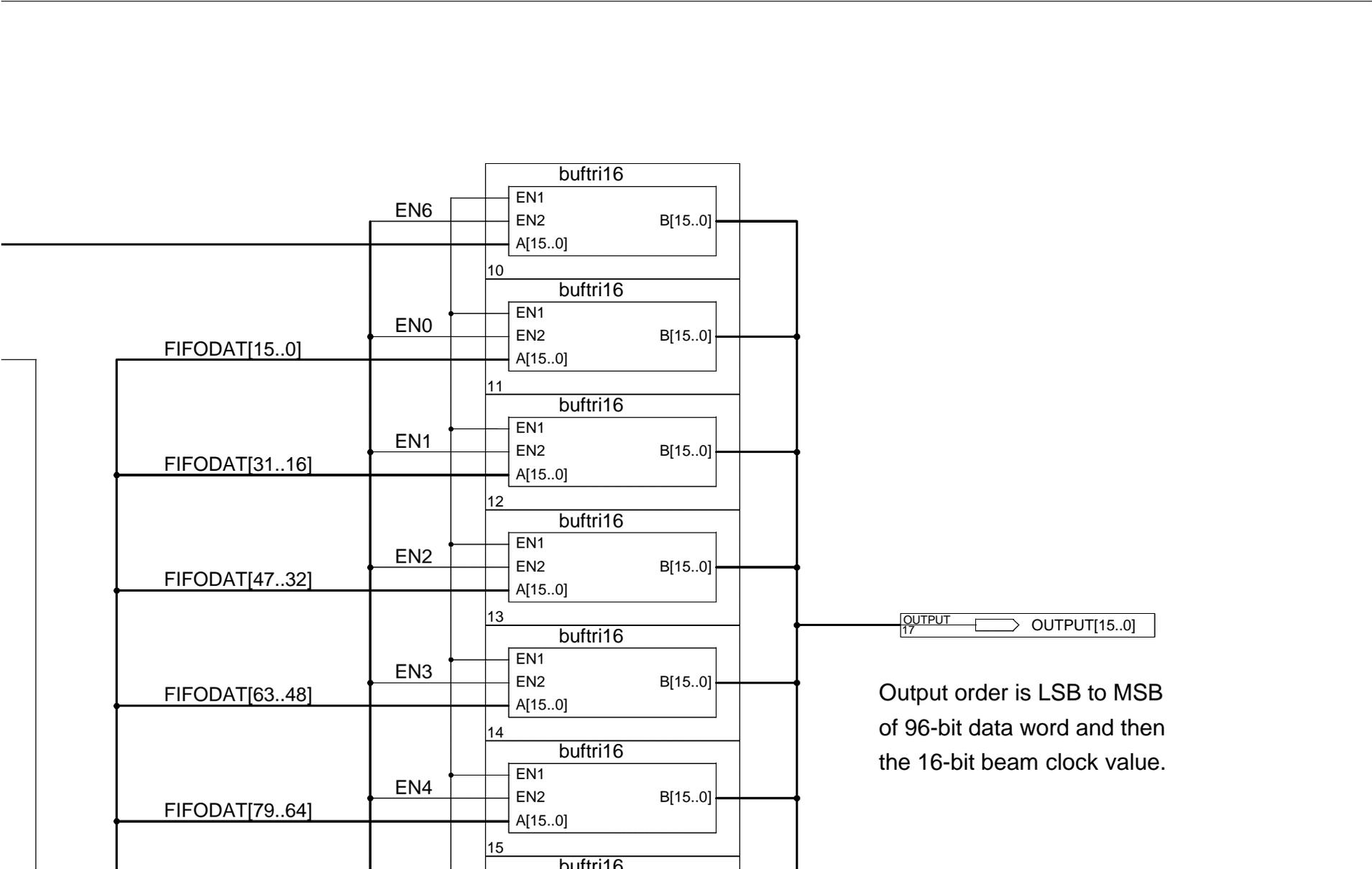
FIFO_EMPTY INPUT

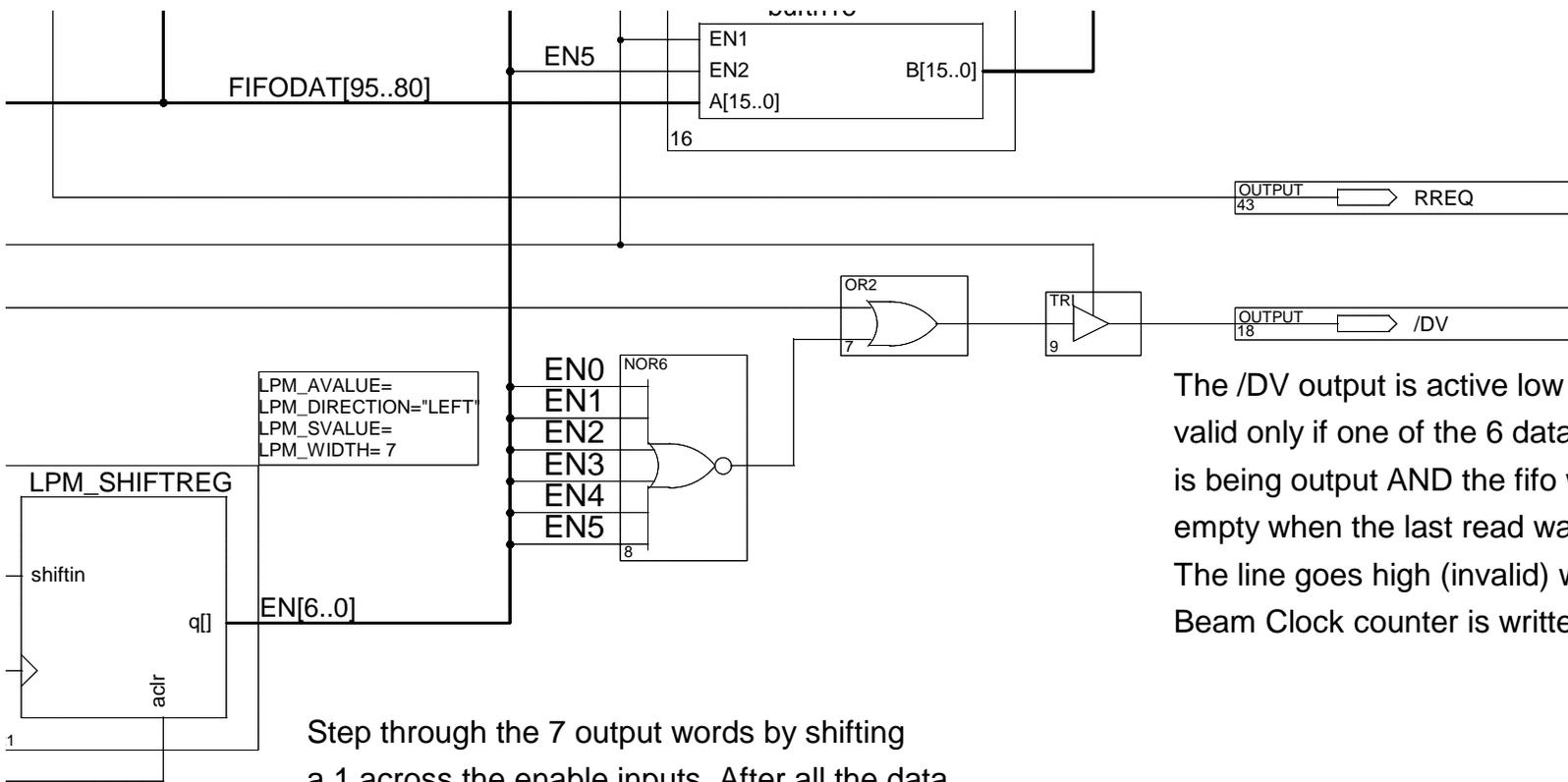
BCLK INPUT

RREQ

Generate a Read Request (RREQ) from a falling edge on /RDEN. Then clear after the FIFO read is performed. Also read the FIFO "empty" flag and store.







The /DV output is active low and valid only if one of the 6 data words is being output AND the fifo was not empty when the last read was performed. The line goes high (invalid) when the Beam Clock counter is written out.

Step through the 7 output words by shifting a 1 across the enable inputs. After all the data is read, the bus is tri-stated. If not all of the data is read, the next read cycle overwrites the data.

TITLE		ReadBlock - Read data from 5-event FIFO		
COMPANY		ORNL		
DESIGNER		Ganesh S. Rao		
SIZE	D	NUMBER	1.00	REV A
DATE	4:37p 3-17-1998	SHEET	1	OF 1
34				