



PHENIX 5-wire serial communication cell (actually has 6 wires).

When RDBACK is low and SCLK pulses, serial data is fed through the circuit. When SLATCH is pulsed, the serial data is clocked out to the parallel circuits to be read by other parts of the system. When RDBACK is HIGH, the PARDATA or latched data output is selected by the multiplexer. Pulsing SCLK latches this data. Then, after setting RDBACK low, SCLK reads the values out. The serial data output is given on SDOUT. /CLR only clears the serial registers and not the parallel output registers.

TITLE	SRLCELL		
COMPANY	ORNL		
DESIGNER	Ganesh S. Rao		
SIZE	B	NUMBER	1.00
REV	A		
DATE	3:26p 12-19-1997	SHEET	1 OF 1
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