The STAR Heavy Flavor Tracker upgrade
STAR Detector

- Coils
- Magnet
- Silicon Vertex Tracker
- E-M Calorimeter
- Time Projection Chamber
- Time Of Flight
- Forward Time Projection Chamber
- Electronics Platforms
Heavy Flavor Tracker Upgrade

ICF
Inner Field Cage

OFC
Outer Field Cage

TPC Volume

HFT

SSD

IST

PXL

Gerrit van Nieuwenhuizen
Hunting the Quark Gluon Plasma

Results from the first 3 years at RHIC
Assessments by the experimental collaborations
April 18, 2005

\[ T \sim 200-400 \text{ MeV} \]
\[ \epsilon \sim 30-60 \epsilon_{\text{nucl}} \]

Perfect liquid

Flows as a relativistic quantum liquid with viscosity to energy density ratio lower than any other known liquid

Highly opaque to colored probes, quarks and gluons, but not to photons

Produces mesons and baryons with yield ratios and flow that suggests formation through quark coalescence from a hot thermal bath
Non zero elliptic flow of electrons from heavy quark decay

Indicative for early thermalization

Expect significant Bottom contribution

Need direct topological reconstruction of heavy quark hadrons

Suppression of electrons from heavy quark decay

Same as for light hadrons >6Gev/c

Heavy quark in-medium energy loss?

Need direct topological reconstruction of heavy quark hadrons
HFT/Detector

2 active PiXeL layers

Intermediate Silicon Tracker

Silicon Strip Detector

- PXL
- IST
- SSD
- TPC
Large drift volume with MWPC readout sectors
Luminosity is up a factor of 3 compared to 2008 pp200 run, and expected to go up 4x in coming years.

Trigger rates can now go up a factor of 3 or more.

pp500 Multiplicities are 1.25x higher than in pp200.

So we are working with ~5x more charge in the TPC than ever before and STAR may ask for ~40x before we are done.
TPC/TipToeing towards RHICII

The STAR TPC is an indispensable 'work horse' for the HFT

Run9: many anode trips due to too much charge and high trigger rates
- leads to unacceptable recovery downtime
- long term wire aging
- short term electronics failures

Mitigation:
- Reduce the gain by 2/3, no negative effect because new electronics has increased S/N from 20:1 to 30:1
- Limit the trigger rate
- Limit the luminosity

Real future meltdown:
- Switch off inner sectors (and let SSD and IST take over)
- Replace anode wires (can be done at high cost)
- Replace MWPC technology by GEM (even higher cost and R&D)

We must choose which options to pursue with care and wisdom
HFT/SSD/Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSD Radius</td>
<td>22 cm</td>
</tr>
<tr>
<td>SSD Sensitive Length</td>
<td>67 cm</td>
</tr>
<tr>
<td>$</td>
<td>\eta</td>
</tr>
<tr>
<td>Number of ladders</td>
<td>20</td>
</tr>
<tr>
<td>Number of wafers/ladder</td>
<td>16</td>
</tr>
<tr>
<td>Total # of wafers</td>
<td>320</td>
</tr>
<tr>
<td># of strips/wafer side</td>
<td>768</td>
</tr>
<tr>
<td># of sides/wafer</td>
<td>2</td>
</tr>
<tr>
<td>Total # of channels</td>
<td>491520</td>
</tr>
<tr>
<td>Silicon wafer size</td>
<td>$75 \times 42 \text{ mm}$</td>
</tr>
<tr>
<td>Silicon wafer sensitive size</td>
<td>$73 \times 40 \text{ mm}$</td>
</tr>
<tr>
<td>Silicon thickness</td>
<td>300 $\mu\text{m}$</td>
</tr>
<tr>
<td>Strip pitch</td>
<td>95 $\mu\text{m}$</td>
</tr>
<tr>
<td>Stereo Angle</td>
<td>35 mrad</td>
</tr>
<tr>
<td>$r$-$\phi$ resolution</td>
<td>20 $\mu\text{m}$</td>
</tr>
<tr>
<td>$z$ resolution</td>
<td>740 $\mu\text{m}$</td>
</tr>
</tbody>
</table>
HFT/SSD/Improvements

Make readout speed compliant with DAQ1000
- parallelize digitization
- increase sampling speed
- increase data transfer speed and use buffers
→ 9% dead at 500Hz (old dead time ~ 60–70%)

Tiling instead of castellating the ladders
- improves hermiticity
- all ladders at same radius and tilt angle
- simplifies mechanical design

Improve reliability of air cooling
- use more rigid air lines to prevent squashing
- air suction from East side only
- use higher capacity 'vacuum cleaner'

SSD easily survives >10 years of 500GeV p+p
- 3.5 krad/year for 500GeV p+p at R=22cm
- rad limit is about 200 krad, mainly readout chip
- **Acceptance:**
  - $-1.2 < \eta < +1.2$ (97.8% spatial coverage)

- **Radiation length:**
  - < 1.5%

- **Readout speed:**
  - Resolve RHIC beam bunch crossing (107ns)

- **Radiation load:**
  - Survive 10 years of RHIC operation: ~30kRad/year

- **Hit requirements:**
  - < 2% occupancy
  - < 1% double hit probability

- **1-layer IST system**

- **Conservative choice** of complete layout

- **Hybrid:** Kapton-based / Carbon-fiber support material

- **Ladders:** Profit from ATLAS experience

- **Sensors:** Silicon pad sensors - Well proven technology and understood / LNS experience

- **FEE:** Based on APV25-S1 chip
  - Basic Hybrid design exists

- **DAQ:** Profit from parallel FGT readout system development
Choice of radius of $r=14\text{cm}$ yields optimized single track efficiency / Fairly insensitive to single track efficiency

- Silicon pad structure preferred over silicon strip layout to reduce amount of double-hit fraction in central Au-Au collisions at 200GeV CME (700 particles per unit rapidity)
- Occupancy for silicon pad layout is $\sim 2\%$ at $r=14\text{cm}$
6 APV chips per sensor (768 channels) yields excellent efficiency with (without) SSD of 83% (73%)

In comparison: 50% for TPC

Efficiency relatively insensitive to changes in number of readout chips and layout of silicon pad sensors
Module:

- 2 Silicon-pad sensors (Double-metal layer, AC coupled) 7.69cm X 4.0cm
- Light-weight Hybrid (Kapton-based / Carbon-fiber support material)
- Readout Chip: APV25-S1

Silicon-pad sensor

- Pad size structure: 6275μm X 596μm
- 6 APV-S1 chips per sensor

APV25-S1 Readout Chips

Conservative technology
Multiple vendors (quote from Hamamatsu)
Expertise and labs at MIT-LNS

(Example: PHOBOS silicon pad sensor)
**HFT/IST/Radiation_Length**

- **Averaged radiation length over 5.3cm width:** ~1.2% $X_0$

<table>
<thead>
<tr>
<th>Component</th>
<th>Radiation Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout chip</td>
<td>0.049%</td>
</tr>
<tr>
<td>CF honeycomb</td>
<td>0.060%</td>
</tr>
<tr>
<td>Cu traces hybrid/cable</td>
<td>0.18%</td>
</tr>
<tr>
<td>CF skin + glue</td>
<td>0.11%</td>
</tr>
<tr>
<td>CF skin + glue</td>
<td>0.11%</td>
</tr>
<tr>
<td>Carbon-Carbon core</td>
<td>0.23%</td>
</tr>
<tr>
<td>Silicon sensor</td>
<td>0.24%</td>
</tr>
<tr>
<td>Cooling water</td>
<td>0.05%</td>
</tr>
<tr>
<td>Al cooling tube</td>
<td>0.08%</td>
</tr>
<tr>
<td>Kapton</td>
<td>0.07%</td>
</tr>
</tbody>
</table>
HFT/IST/Prototypes

- 4 PHOBOS 512 channel pad sensors
- 16 APV25-S1 readout chips
- 75μm thick Kapton hybrid with 60cm long tail - Assembled at MIT
- Wire bonded at BNL's Instrumentation Division
- 2 prototypes have been assembled
- 1 partially bonded prototype currently being tested
- Don Pinelli waiting for fine pitch bonding tools
HFT/IST/Readout_Chip

- Developed for CMS (75000 in CMS tracker) and also used by COMPASS for triple-GEM detector readout
- 0.25μm CMOS
- 128 channels
- 40 MHz sampling rate
- 4μs analogue pipeline
- 11:1 Signal / Noise
- 0.3 Watt / chip
- Radiation hard

- 'Off-the shelf' readout chip: APV25-S1
- Used for STAR IST, FGT and pp2pp (1 readout system)!
First prototypes of ARM/ARC system ready May/June 2010.
- Prototype ladder produced at LBNL: Carbon fiber honeycomb with carbon fiber skins (80cm / Current design is 50cm)
- 1 cooling channel
- Prototype ladder support rapid prototyped
- Support mechanism: Click-in / Lock-in of ladders
### HFT/PXL/Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pointing resolution</td>
<td>(13 $\oplus$ 22 GeV/p-c) $\mu$m</td>
</tr>
<tr>
<td>Layers</td>
<td>Layer 1 at 2.5 cm radius</td>
</tr>
<tr>
<td></td>
<td>Layer 2 at 8 cm radius</td>
</tr>
<tr>
<td>Pixel size</td>
<td>18.4 $\mu$m x 18.4 $\mu$m</td>
</tr>
<tr>
<td>Hit resolution</td>
<td>10 $\mu$m rms</td>
</tr>
<tr>
<td>Position stability</td>
<td>6 $\mu$m (20 $\mu$m envelope)</td>
</tr>
<tr>
<td>Radiation thickness per layer</td>
<td>$X/X_0 = 0.37%$</td>
</tr>
<tr>
<td>Number of pixels</td>
<td>$\sim 436$ M</td>
</tr>
<tr>
<td>Integration time (affects pileup)</td>
<td>0.2 ms</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>300 kRad</td>
</tr>
<tr>
<td>Rapid installation and replacement to cover radiation damage and other detector failure</td>
<td>Installation and reproducible positioning in 8 hours</td>
</tr>
</tbody>
</table>
- Standard commercial CMOS technology
- Room temperature operation
- Sensor and signal processing are integrated in the same silicon wafer
- Signal is created in the low-doped epitaxial layer (typically ~10-15 μm) → MIP signal is limited to <1000 electrons
- Charge collection is mainly through thermal diffusion (~100 ns), reflective boundaries at p-well and substrate → cluster size is about ~10 pixels (20-30 μm pitch)
- 100% fill-factor
- Fast readout
- Proven thinning to 50 micron
Complementary detector readout

- Pixel Sensors
  - analog signals
- ADC
  - digital
- CDS
  - analog signals
- CDS
  - digital signals
- Disc.
- Data sparsification
- readout to DAQ

1. MimoSTAR sensors
   - 4 ms integration time
2. Phase-1 sensors
   - 640 μs integration time
3. PXL final sensors (Ultimate)
   - < 200 μs integration time
Last phase → Ultimate sensor

- Overall design is in progress and nearly complete.
- 18.4 μm pixels have been chosen for enhanced radiation tolerance.
- Triggered detector system fitting into existing STAR infrastructure (Trigger, DAQ, etc.)
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (1 kHz for DAQ1000).
- Have live time characteristics such that the Pixel detector is live whenever the TPC is live.
- Reduce the total data rate of the PXL detector to a manageable level (< TPC rate of ~1MB / event).
Easy to reconfigure FPGA firmware to adapt to final sensors
Maintain a 20um internal calibration → Lots of simulations and material tests are on the way
HFT/Support

MSC assembly: 19.8 kg
SSD: 3 kg each
GEM disks: 13.5 kg total

Weight: \(~35 \text{ kg}\)

\(~0.5\text{mm} \text{ Deflection}\)
HFT/Stability

- Stability of IDS not critical for HFT unless Beam Constraint used (100μm)
- It is critical for FGT—FGT is intimately involved in design of IDS
- Gravity Sag can be used to project RMS Stability
  - 0.5mm sag has $F_0 \sim 20$Hz
- For Given PSD, Vibration is <10μm RMS
- IDS easily meets this requirement as designed
Because of the thin pixel layers the HFT will be able to measure down to $p_T \sim 0.5$ GeV/c.
500M minimum bias events with induced D0 flow from cascade model
Tracked through STAR with the HFT upgrade

Flow $\rightarrow$ Thermalization of light-quarks

No Flow $\rightarrow$ Drag coefficients

HFT will allow for precision measurements to address questions with respect to thermalization and in-medium effects
HFT/Suppression

500M minimum bias events from cascade model, D0 suppressed like light flavor
Tracked through STAR with the HFT upgrade

Significant contribution of electrons from bottom decay
Topological reconstruction of D0 necessary

HFT will allow for precision charm measurements to address questions with respect to collisional and radiative effects
Waiting for the latest physics predictions before planning CD-2

Gerrit van Nieuwenhuizen
### Pixel Project Profile

<table>
<thead>
<tr>
<th>Year</th>
<th>Contingency</th>
<th>Low Range</th>
<th>High Range</th>
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<tbody>
<tr>
<td>2011</td>
<td>$50,000</td>
<td>$90,000</td>
<td>$120,000</td>
</tr>
<tr>
<td>2012</td>
<td>$190,000</td>
<td>$420,000</td>
<td>$590,000</td>
</tr>
<tr>
<td>2013</td>
<td>$520,000</td>
<td>$1,400,000</td>
<td>$1,800,000</td>
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<tr>
<td>2014</td>
<td>$570,000</td>
<td>$1,800,000</td>
<td>$2,300,000</td>
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### Contingency Overview

<table>
<thead>
<tr>
<th>WBS</th>
<th>Title</th>
<th>Cost</th>
<th>Contingency %</th>
<th>Contingency $</th>
<th>Low Range</th>
<th>High Range</th>
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<tbody>
<tr>
<td>1.1</td>
<td>Project Management</td>
<td>1002</td>
<td>9%</td>
<td>90</td>
<td>1047</td>
<td>1124</td>
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<tr>
<td>1.2</td>
<td>Pixel</td>
<td>4780</td>
<td>32%</td>
<td>1540</td>
<td>5550</td>
<td>6859</td>
</tr>
<tr>
<td>1.3</td>
<td>Intermediate Silicon Tracker (IST)</td>
<td>2650</td>
<td>36%</td>
<td>960</td>
<td>3130</td>
<td>3946</td>
</tr>
<tr>
<td>1.4</td>
<td>Silicon Strip Detector (SSD)</td>
<td>660</td>
<td>44%</td>
<td>290</td>
<td>805</td>
<td>1052</td>
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<tr>
<td>1.5</td>
<td>Integration</td>
<td>1380</td>
<td>43%</td>
<td>600</td>
<td>1680</td>
<td>2190</td>
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<tr>
<td>subtotal</td>
<td></td>
<td>10472</td>
<td>33%</td>
<td>3480</td>
<td>12212</td>
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<td>Contributed Labor</td>
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<td>2345</td>
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<tr>
<td>Total Project Cost</td>
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<td>12817</td>
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<td>3480</td>
<td>14557</td>
<td>17515</td>
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### HFT/Schedule

<table>
<thead>
<tr>
<th>Milestone</th>
<th>Date</th>
<th>Milestone Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receive Prototype Sensors from IPHC</td>
<td>Q3</td>
<td>FY10 Review of board layout for ladder board and RDO</td>
</tr>
<tr>
<td>Pixel Prototype Sector Design Complete</td>
<td>Q2</td>
<td>FY11 Finish testing ladder board @BNL (digital event processing only). Finish testing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RDO @BNL. Integrated testing @ Subatech for both boards</td>
</tr>
<tr>
<td>Prototype Insertion mechanism Testing Complete</td>
<td>Q3</td>
<td>FY11 Develop slow controls and DAQ software</td>
</tr>
<tr>
<td>Receive final Ultimate Sensors from IPHC</td>
<td>Q4</td>
<td>FY12 Produce full complement of boards</td>
</tr>
<tr>
<td>Sector Assembly start</td>
<td>Q4</td>
<td>FY13 Move Full System to STAR for test</td>
</tr>
<tr>
<td>PXL detector available for insertion</td>
<td>Q3</td>
<td>FY13 Install completed SSD in STAR</td>
</tr>
</tbody>
</table>

**Planning to be ready for Run 14**
HFT upgrade essential to extend STAR HI physics to heavy flavor sector

All components of HFT have been defined through Conceptional Design Report

All components of HFT are still on schedule, but slow funding is becoming an issue

Waiting for CD-1, preparing for CD-2/3